

# Real-Time One-Way Flight Communications

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## Introduction

In this project we are designing a flight computer for amateur rocketry. One of its features will be the ability to transmit data during the flight wirelessly to a ground computer. This is known as data-downlink, because the data is sent “down” to Earth from the rocket. This computer must operate in real-time to maintain data accuracy, meaning data-downlink must be a low-latency operation. First data must be packetized for transmission, then a carrier signal is modulated and put on a high-frequency carrier, which is then received by the ground station computer, demodulated, and the data is read.

## Hardware for Serial Communications

### Introduction to UART

The algorithm the flight computer uses to calculate position, velocity, and attitude involves many matrix operations.<sup>1</sup> These are computationally expensive, and depend on time, meaning the computer has little time to perform IO operations. Another issue is that different transmitters have different interfaces for receiving the data to transmit. To add flexibility, it makes sense to split the workload between two computers: one that does the calculations, and one that performs communications. The immediate issue presented is how to send the calculation results from one computer to the other and do so in an efficient manner. Most boards come with a *universal asynchronous receiver-transmitter* (UART), which, as the name suggests, provides a non-blocking method of serial communication. It is actually a circuit, instead of a protocol.<sup>2</sup> Note there is also USART, which supports a synchronous mode that is slightly faster, however UART is more common.

### UART Implementation

UART involves two pins for transmitting and receiving, TX and RX. The transmission pin of one board is connected to the receiver of the other. The data to be transmitted is loaded into a shift-register reserved by the UART. The system is asynchronous because the transmitter and receiver do not share a clock signal. Instead, a start and stop bit is added so the receiver knows when to start and stop reading. The transmitter serially outputs the start bit, followed by the data bits in the buffer, and finally the stop bit.<sup>2</sup> Therefore, UART performs parallel-to-serial conversion. This process happens independently of the software program, meaning the software is free to perform other tasks.

### Interfacing UART with Software

Two important parameters are the baud rate (transmitted bits/s), and the buffer’s available space. The baud rate must be matched between boards, otherwise data may be misread. The buffer capacity is especially important for this application. If the software attempts to write more data to the buffer than it has available, the present data may be overwritten or corrupted. Alternatively, in some library functions the program waits until enough space is available- a blocking operation that wastes time and must be avoided here. Therefore, the buffer’s available space should always be checked before writing to it. Most boards come with a library function to do this. On the receiving side, there is another buffer for storing the received data, so the software does not need to read it continuously. However, the software should read often enough so that this buffer does not fill.<sup>2,3</sup>

## Modulation Techniques

Now that the data is on the other computer, the next step is to transmit it. This involves two main steps: converting the bits into an analog signal (the message signal), and then putting the message signal on a high frequency carrier wave. The most common modulation techniques used in data-downlink are Phase-Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM)<sup>4</sup>, a type of Amplitude-Shift Keying (ASK)<sup>5</sup>. Some important considerations are ease of implementation, the bit-error rate (BER), and the data-rate.<sup>5</sup> The simplest modulation technique is On-Off Keying (OOK), a type of binary ASK. On a typical microcontroller, a 0 bit is mapped to 0V, and a 1 bit is mapped to 5V or 3.3V (depending on the logic the board uses), generating a series of rectangular pulses. The pulse or pulses that represent a bit sequence is called a symbol. Since every microcontroller is capable of digital output, implementing this method is as easy as asserting high or low on a pin at regular intervals. The downside is that it is susceptible to additive white-gaussian noise (AWGN) and has a low data-rate since it only transmits one bit at a time.<sup>6,7</sup>

### Phase-Shift Keying

PSK modulates the phase rather than amplitude, so it is less susceptible to AWGN. The common types of PSK used in data-downlink are Quadrature PSK (QPSK), Offset QPSK (OQPSK), and 8PSK.<sup>5</sup> QPSK transmits both a cosine and sine wave, each carrying a bit. While PSK modulates the phase of a single carrier wave, using trigonometric identities it may be written as the amplitude modulation of a cosine and a sine. The cosine is the “in-phase” component and the sine is the “quadrature” component. In this way a bit may be placed on each and, by transmitting both carriers, transmit two bits at once. The reason this works is that cosine and sine are 90 degrees phase shifts of each other, so they are “orthogonal” (i.e., they do not correlate), so the two do not interfere with each other at the transmitter or receiver. This already has the advantage of a higher data-rate than OOK. However, two bits requires four different symbols rather than two (using the full range of B bits requires  $2^B$  different symbols).<sup>x</sup> Furthermore, QPSK has a better BER than OOK, so it is mostly an upgrade.<sup>x</sup> However, the power requirement is doubled since each symbol requires two pulses.

### Quadrature Phase-Shift Keying

QPSK may have phase shifts up to 180 degrees, which can cause large variations in amplitude. To overcome this issue, a variation called Offset QPSK (OQPSK) has been developed. By adding a delay of one bit period between bits, the phase shift is limited to 90 degrees, and the amplitude does not vary as sharply.<sup>8</sup> However, this added delay slows transmission so it may not be desirable. To transmit at even higher bit rates, QAM is preferred over PSK. Despite the name, it is actually a mix of amplitude and phase modulation. The equation for it is identical to QPSK, except now the modulation amplitude may vary arbitrarily (whereas before it varied according to the phase). In QPSK, since only the phase changes every symbol has the same energy. If plotted on a symbol constellation, it forms a circle. This is not the case in QPSK, where the symbol energy may vary, and consequently the symbol constellation can form any arbitrary shape and is a design choice. It is typical to choose the constellation in a way that minimizes the average symbol energy.

### Quadrature Amplitude Modulation

When doing QAM, the number of different symbols is almost always chosen as a power of two, since they make full use of the available bits. The symbol constellation may be anything, but rectangles are common since they are easy to construct and easy to demodulate. In the special case of two bits (4QAM), the system is identical to QPSK (including BER). The advantage of QAM over PSK is that symbols may be placed farther apart in the constellation, which reduces the BER. In PSK, all symbols are constrained to a circle, so as the number of symbols increases the spacing decreases and bit errors are more likely to occur.<sup>5</sup> The most common forms of QAM in data-downlink are 16QAM and 32QAM.<sup>4</sup> Demodulating either scheme involves first multiplying the received signal by the carrier frequency (this shifts it back to baseband), and then passing it through a matched filter or correlator filter. These filters are the optimal filters for removing additive white gaussian noise. The impulse response of both filters is a shifted and flipped version of the original modulation pulse. The oscillators generating the carrier frequency at the transmitter and receiver will never have the same phase, so phase tracking is necessary and typically

accomplished using a phase-locked loop (PLL). At the output, QPSK simply checks the phase and declares the closest symbol as the received symbol. QAM is a little more involved since it must compute the distance of the received symbol to all other symbols in the constellation and choose the closest one as the received symbol.<sup>4</sup>

### **Phase-Locked-Loop**

A PLL is a negative-feedback system to automatically minimize phase error. It works by using a phase-comparator to generate an error signal, and then using it to drive a voltage-controlled oscillator that produces a signal with the corrected phase. The output signal is fed back to the input of the phase-comparator, forming the loop.<sup>9,10</sup> An order-two transfer function is reasonably effective and is realizable through capacitors and resistors.<sup>10</sup> It is also possible to implement this system digitally

or hybrid<sup>9</sup>, but this adds complexity and will not be used here. Some receivers will use different methods of demodulation to avoid needing a PLL, however they suffer from a high BER and since this system needs to work over long distances these methods will not be employed.

Once the signal is demodulated and the bits recovered, it is a simple matter to convert the bit series back to the original data. The two systems must be in agreement on how many bits define a piece of data, e.g. if an integer is four bytes then every 32 bits is an int, and the computer is then free to process the data. Much of the complexity of design may be alleviated through the use of integrated circuits (IC's) or readily available transmitter/receiver pairs.



Figure 1. *Curabitur pharetra iaculis mauris, a consectetur odio fermentum sed*

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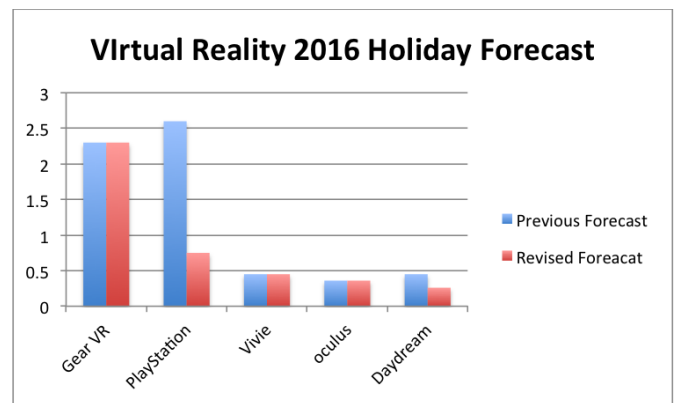


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### **Conclusion**

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