A 32 × 32 Capacitive Micromachined Ultrasonic Transducer Array Manufactured in Standard CMOS

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***Abstract*—As ultrasound imagers become increasingly portable and lower cost, breakthroughs in transducer technology will be needed to provide high-resolution, real-time 3-D imaging while maintaining the affordability needed for portable systems. This paper presents a 32 × 32 ultrasound array prototype, manufactured using a CMUT-in-CMOS approach whereby ultrasonic transducer elements and readout circuits are integrated on a single chip using a standard integrated circuit manufacturing process in a commercial CMOS foundry. Only blanket wet-etch and sealing steps are added to complete the MEMS devices after the CMOS process. This process typically yields better than 99% working elements per array, with less than ±1.5 dB variation in receive sensitivity among the 1024 individually addressable elements. The CMUT pulse-echo frequency response is typically centered at 2.1 MHz with a −6 dB fractional bandwidth of 60%, and elements are arranged on a 250 μm hexagonal grid (less than half-wavelength pitch). Multiplexers and CMOS buffers within the array are used to make on-chip routing manageable, reduce the number of physical output leads, and drive the transducer cable. The array has been interfaced to a commercial imager as well as a set of custom transmit and receive electronics, and volumetric images of nylon fishing line targets have been produced.**

I. Introduction

The shrinking size, cost, and power consumption of ultrasound system electronics is enabling widespread deployment of portable and handheld imaging systems. Front-end low-noise amplification (LNA), time-gain compression (TGC), and analog-to-digital conversion (ADC) functions that previously required stacks of custom printed circuit boards are now being delivered as off-the-shelf solutions that accomplish these tasks within a single chip or single package, even with four, eight, or more channels per package [1], [2]. Likewise, digital filtering, beamforming, scan conversion, image processing, and user-interface tasks can now be performed quickly, compactly, and cheaply by highly integrated digital electronics [(including digital signal processors (DSPs) and field-programmable gate arrays (FPGAs)], which benefit from the Moore's-law-driven trends of the semiconductor industry in computational speed, density, and cost. As medical imaging products continue to reap these benefits, and as integration levels advance using the system-on-chip and system-in-package technologies detailed elsewhere in this issue, high-quality 3-D/4-D imaging will likely be within reach even for portable imagers.

An important exception to the rule that ultrasound imaging will improve based on advances in electronics is found in transducer array technology. Ultrasound arrays provide the critical interface between the inherently mechanical information source (acoustic echoes from human tissue) and the electronic hardware that captures and presents image data to users. Conventional piezoelectric technology's suitability as an interface is becoming stretched by demands for higher image quality and more complex array configurations. As examples, high-frequency imaging requires precisely machined thin substrates [3], broad bandwidth demands complex matching layers [4], invasive intravascular and endoscopic imaging benefits from irregular array geometries [5]–[7], and electronically steered 3-D imaging requires dense 2-D arrays with many elements [8]–[10]. Capacitive micromachined ultrasonic transducer (CMUT) technology emerged in the 1990s [11]–[14], providing a potential solution for meeting these demands by improving the flexibility and imaging quality of ultrasound arrays using micro electromechanical systems (MEMS) technology to build transducer elements directly on silicon substrates.

A MEMS approach means that transducer arrays can be created in batch quantities using integrated circuit processing steps rather than relying on mechanical dicing of individual array elements using conventional machining. Element dimensions are defined laterally by photolithography with submicron precision, and vertically by tightly controlled vacuum-deposited thin-film layers (for surface-micromachined devices). The potential advantages of CMUTs have become well known. These include broad bandwidth performance due to less impedance mismatch between tissue and the thin transducer diaphragms [4], [15], the ability to create small elements with high center frequencies, design freedom for 2-D arrays and non-orthogonal array geometries [6], [16], and the capacity

Manuscript received May 15, 2011; accepted April 20, 2012. This work was supported by the National Science Foundation Small Business Innovation Research/Small Business Technology Transfer Program under Award No. 0450493.

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DOI http://dx.doi.org/10.1109/TUFFC.2012.2352

for integrating circuits on the same silicon substrate [17], [18]. Tight coupling between electronics and ultrasound transducer elements is desirable for many reasons that commonly motivate system-on-chip integration in other applications, including signal integrity, component count, assembly costs, and system size. In ultrasound, a high level of integration is especially attractive for large-scale planar 3-D/4-D imaging arrays, which need vulnerable signals to be routed out from a huge number of densely packed elements (e.g., 16 384 elements at 200 to 300 μm pitch for a 128 × 128 abdominal imaging array). Locating amplifiers on chip as close as possible to the elements maximizes the signal-to-noise ratio. Using multiplexers to combine signals from multiple elements reduces the quantity of physical output lines to a reasonable number. Although these functions are the most essential to integrate immediately at the array, some applications could benefit from also integrating high-voltage transmit pulsing, receive signal filtering, TGC, and ADC functions on chip or within the probe handle [8], [18].

Several successful approaches have been demonstrated for closely integrating CMOS electronics with CMUT elements: 1) using through-silicon vias (TSV) to carry CMUT signals through the substrate to a ball-bumped circuit substrate below [19], [20]; 2) depositing/patterning CMUT layers over the top of CMOS circuits, connecting the elements to circuits by aligning CMUT contacts to underlying CMOS pads [18], [21], [22]; and 3) using the layers of the CMOS circuit itself as the structural layers of the CMUT, typically by inserting CMUT-related process steps into the circuit fabrication sequence [17], [23], [24].

The CMUT-in-CMOS approach presented in this paper is most closely related to the third strategy above; however, a special emphasis is placed on maintaining the integrity of the CMOS process itself, such that an unaltered foundry CMOS process flow can be used to produce the CMUT structures alongside circuits. After the CMOS process is complete, chips or wafers are subjected to only two additional steps, a sacrificial etch and a dielectric deposition, neither of which requires additional photolithography (although a noncritical photoresist patterning step could be added to protect bonding pads for release etching at the wafer level). This approach is motivated by the idea that affordability and reliability are best maintained by using high-volume batch manufacturing. In contrast to some high-volume MEMS products such as automotive/gaming/communications components, ultrasound transducers are typically sold in relatively low quantities (<10 000 per year). This means that developing and maintaining a custom nonstandard manufacturing process could impose very high per-part costs for probes. To keep probes affordable, it is advantageous to instead leverage a standardized high-volume manufacturing process. Therefore, the arrays reported here use a CMUT fabrication approach based on standard CMOS manufacturing, which benefits from the staggering economies of scale enjoyed by products in the semiconductor industry.

This paper presents the design, fabrication, and characterization of a fully populated 32 × 32 ultrasound array fabricated using the CMUT-in-CMOS approach illustrated in Fig. 1. This work provides an initial demonstration of the feasibility of using a CMOS-based fabrication process to realize high-element-count 2-D arrays for 3-D imaging. It also provides a practical example of the benefits of moving toward a system-on-chip level of integration within ultrasound systems, and in this case, even within the imaging array.

II. Methods

A. CMUT-in-CMOS Element Design

The CMUT-in-CMOS approach for realizing integrated transducer devices is illustrated in Fig. 1. For the array presented here, the manufacturing process was based on a mature 1.5-μm mixed-signal CMOS fabrication process [25], [26] with two metal layers and two polysilicon layers,

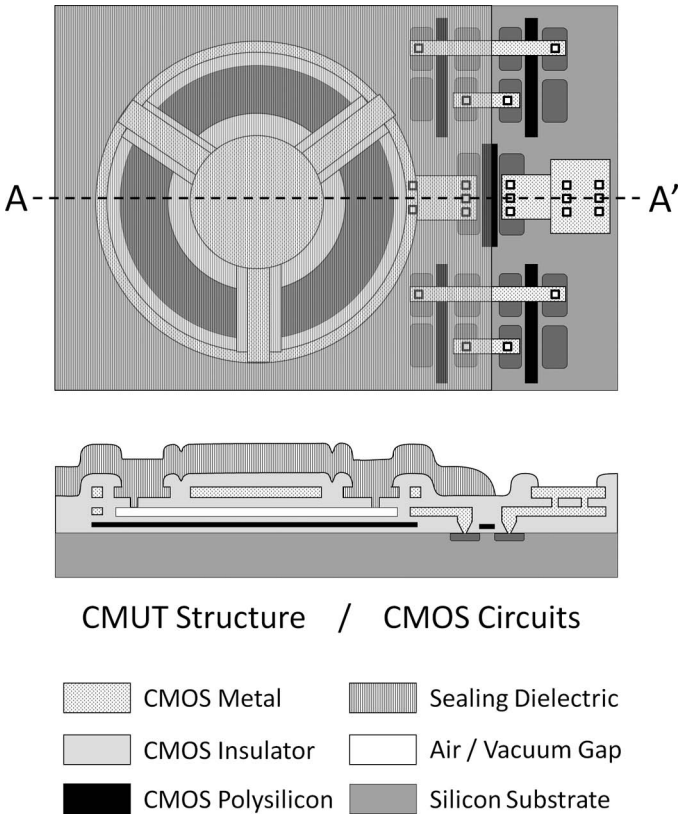

Fig. 1. The CMUT-in-CMOS concept whereby MEMS transducer elements are formed using the metallization and passivation layers of an unaltered CMOS foundry process. The lower drawing shows a cross-section of the device taken along line A-A′ in the upper drawing. To increase membrane flexibility, the CMUT elements have a support rim that is thinner than the central region. In this first implementation, the CMOS circuits reside side by side with the CMUTs, which results in a somewhat low fill factor. This can be addressed in the future by using a CMOS process with more metal layers, such that the layers used for MEMS can reside directly above electronic components and routing lines.

TABLE I. CMUT ELEMENT AND ARRAY DESIGN PARAMETERS.

Parameter	Value	Comment
Target center frequency	1 to 4 MHz	General abdominal imaging
CMUT/electrode diameter	100 μm/60 μm	One CMUT per element
Mechanical gap	0.6 μm	Set by CMOS metal layer thickness
Membrane rim thickness	1.0 μm	Prior to sealing layer deposition
Central membrane thickness	3.4 μm	Prior to sealing layer deposition
Sealing layer thickness	1.5 to 3.0 μm	PECVD Oxynitride or Parylene-C
Number of elements	1024	32 × 32 arrangement on hex grid
Receive element pitch	250 μm	λ/2 hex grid to avoid grating lobes
Transmit cluster pitch	500 × 900 μm	Clusters of 2 × 4 elements on TX

although more advanced processes can be also be used. As shown in the cross-sectional drawing in Fig. 1, the metal, polysilicon, and dielectric layers of the CMOS fabrication process form key components of both the mechanical transducer element and the adjacent readout circuitry. Specifically, the two CMOS interconnect metals form the upper CMUT electrode and the sacrificial layer, respectively. The polysilicon gate layer of the CMOS process forms the lower electrode of the CMUT. The dielectric passivation layers within the circuit constitute the transducer membrane itself and insulate the CMUT electrodes from each other and the environment. The sharing of layers for CMUTs and transistors enables CMOS circuits and CMUT elements to be fabricated side by side on the same chip. To increase the element fill-factor, higher level metal and dielectric layers could be used for the CMUT structure, allowing circuit elements to reside beneath the mechanical devices.

Each element consists of a single 100-μm-diameter CMUT targeted for the 1 to 4 MHz range of operation, which is well-suited for abdominal imaging. Element and array design parameters are summarized in Table I. The CMUT is designed with a 60-μm-diameter upper electrode, suspended on a dielectric membrane and electrically connected to a contact ring using three "spokes" evenly spaced for mechanical symmetry (see Fig. 1, top). The design was constrained by the CMOS layer thicknesses in the vertical dimension and by foundry design rules in the lateral dimensions. For example, as indicated in Table I, the gap is formed by sacrificing a 0.6-μm-thick lower metal layer, and the upper electrode thickness is dictated by the 1.0-μm upper metal thickness. The CMOS layer thicknesses and material properties are discussed in more detail in [27]. To observe foundry design rules, release holes were limited to 1.5 × 1.5 μm as prescribed for the CMOS vias. As shown, the CMUT diaphragm has a rim region that is thinner than the central electrode region, to facilitate higher membrane compliance [27]. To obtain the thinner rim region without adding fabrication steps, an opening in the CMOS passivation/overglass layer is defined in the layout, and a sacrificial ring of metal is included to adhere to the design rule that requires passivation openings to be fully overlapped by the upper metal layer. During the device release etch step, the metal ring is removed, leaving only the thin support layer below. The upper CMUT electrode is connected to on-chip receive circuits (see Section II-B) by way of the metal spokes and contact ring as illustrated in Fig. 1 (top). The requisite dc bias and transmit signals are applied to the lower electrode, which is isolated from the substrate by a thick oxide layer and from sensitive circuit nodes by several dielectric layers in series with the CMUT vacuum gap. Because these isolation layers have a high dielectric strength, potentials exceeding ±100 V can be applied to the lower plate of the CMUT structure without causing dielectric breakdown or significant leakage current to the upper electrode or to the substrate. For fabrication simplicity (detailed below), a uniform blanket of dielectric material is used to hydrostatically seal the CMUT gap, forming a low-pressure cavity that is protected from intrusion of water or foreign particulate. The thickness and Young's modulus of the sealing material affect the stiffness and mass of the diaphragm, which influence the center frequency and transmit/receive sensitivity of the CMUT. Because this material is deposited after the CMOS foundry steps, deposition parameters can be adjusted to tune CMUT performance specifications.

B. Transducer Element Modeling

The dynamics of the CMUT have been modeled using the approach reported by Doody *et al.* [28], which combines finite element analysis (FEA) with a lumped-element model to achieve good accuracy while maintaining computational efficiency. The lumped-element model is shown as an equivalent circuit in Fig. 2. Table II summarizes the values for the model components, which are acquired using a combination of analytical calculations and finite-element computations as explained in detail elsewhere [28]. The external acoustic environmental loading components R_{A1}, R_{A2}, M_{A1}, C_{A1} are similar to those described by Beranek for a baffled piston [29], but are modified as described by Doody *et al.* [28] to account for the bending modeshape of the CMUT. C_{elect} is the electrostatic spring compliance, which is computed based on a static operating point determined from the applied dc bias, and takes into account the incomplete electrode coverage and bending modeshape. The method has been described in detail in Doody *et al.* [28]. C_{cav} is the cavity compliance, computed using the volume of the gap behind the diaphragm in its statically deflected position. N is the electrostatic coupling between the electrical to the mechanical side,

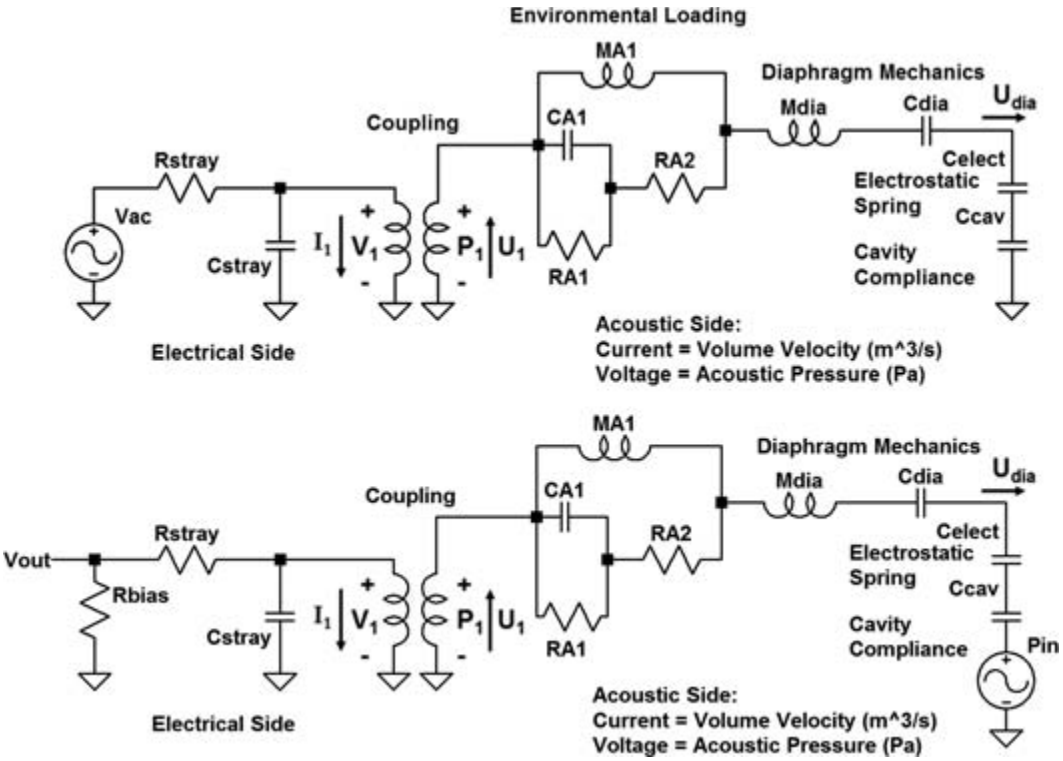

Fig. 2. Lumped element model of the CMUT element in transmit mode (top) and receive mode (bottom). The electrical side of each model is on the left, and the acoustic side on the right.

$$P_1 = N \cdot V_1,$$
$$I_1 = N \cdot U_1,$$

which includes the effects of incomplete electrode coverage and statically deflected gap. Again, the computation of this parameter is fully described in Doody *et al.* [28].

C_{dia} represents the *in vacuo* static volume compliance of the diaphragm, which is the area integral of the displacement under unit applied uniform pressure. M_{dia} represents the effective modal mass of the diaphragm for the first bending mode, which can be computed from the first *in vacuo* modal frequency, ω_1, by

$$M_{\text{dia}} = (\omega_1{}^2 C_{\text{dia}})^{-1}.$$

These parameters were determined by finite element analysis in COMSOL Multiphysics (COMSOL Inc., Burlington, MA). For the structure presented in this paper, the cross-section is not axisymmetric, but varies with angular position according to the spoke structure discussed above. Therefore, to compute the static volume compliance and first modal frequency, a 2-D Mindlin plate model was employed [30] as shown in Fig. 3. In each of the three regions, different thin film layers are present. The layers for each of the three regions are listed, along with the material properties for each layer, in Table III. The flexural stiffness and mass per unit area for each of the three regions is computed by applying classic laminate plate theory. In each region, the position of the neutral axis with respect to the

TABLE II. PARAMETERS FOR LUMPED-ELEMENT CMUT MODEL.

Model parameter	Value	Description
C_{A1}	$9.39{\cdot}10^{-22}$ m^3/Pa	Environmental loading parameter
M_{A1}	$4.09{\cdot}10^{6}$ kg/m^4	Environmental loading parameter
R_{A1}	$5.43{\cdot}10^{13}$ kg/m^{4}s	Environmental loading parameter
R_{A2}	$1.91{\cdot}10^{14}$ kg/m^{4}s	Environmental loading parameter
R_{stray}	1 Ω	Series parasitic resistance
C_{stray}	10 fF	Parallel parasitic capacitance
C_{dia}	$1.72{\cdot}10^{-21}$ m^3/Pa	Volume displacement
M_{dia}	$2.35{\cdot}10^{6}$ kg/m^4	Effective modal mass of the diaphragm for the first bending mode
C_{elect}	$-1.07{\cdot}10^{-17}$ m^3/Pa	Electrostatic spring compliance
C_{cav}	$7.47{\cdot}10^{-16}$ m^3/Pa	Cavity compliance
N	45.9 Pa/V	Electroacoustic coupling factor for 100 V bias
C_b	100 pF	ac coupling capacitor value
R_b	1 MΩ	dc bias resistor
C_L	9.5 pF	Load capacitance
R_L	10 MΩ	Load resistance

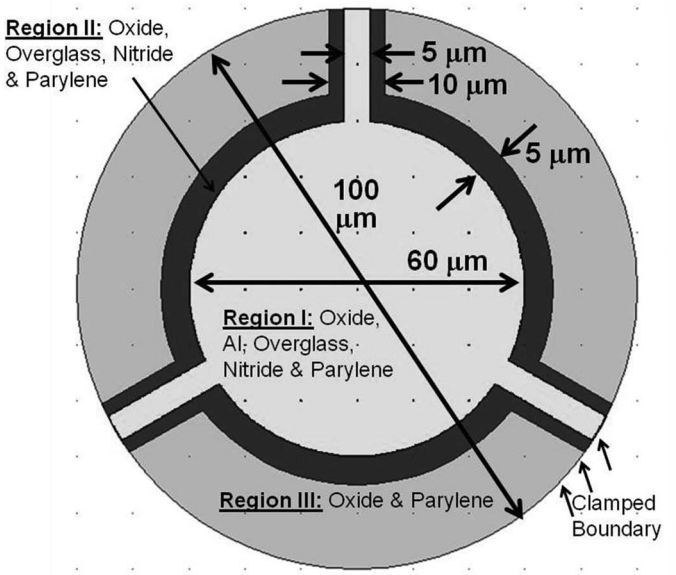

Fig. 3. Diagram showing the Mindlin plate model used for computation of the *in vacuo* structure compliance and modal frequency. The three regions of the plate are made up of different layers, resulting in different flexural stiffness values and mass densities. The layer properties for each region are shown in Table III.

bottom of the plate is computed, where the sum is over the layers that are present in that portion of the plate,

$$y_c = \frac{\sum_{n=1} \frac{y_n E_n t_n}{(1-\upsilon_n^2)}}{\sum_{n=1} \frac{E_n t_n}{(1-\upsilon_n^2)}},$$

where y_n is the position of the center of the nth layer above the bottom of the plate, t_n is the thickness of the nth layer, and E_n and υ_n are the elastic modulus and Poisson ratio of the nth layer. With this in hand, the position of the center of the nth layer with respect to the neutral axis can be computed,

$$z_n = y_n - y_c.$$

Finally, the area moment of inertia of the nth layer is

$$I_n = \frac{t_n^3}{12} + z_n^2 t_n.$$

From this, the total effective flexural modulus can be computed for use in the plate calculation, where the sum is over the layers that are present in that part of the plate,

$$D_{\text{eff}} = \sum_{n=1} \frac{E_n I_n}{(1-\upsilon_n^2)},$$

The mass per unit area is also needed for the modal frequency calculation and is easily determined from the densities and thicknesses of the layers that are present in the region of the plate under investigation,

$$m_a = \sum_{n=1} \rho_n t_n.$$

The thickness and elastic modulus of the seven relevant CMOS process layers were obtained from the careful work of Marshall *et al.* [25], [26]. The Poisson ratios were taken from Laconte *et al.* [31]. The density of Parylene C, 1290 kg/m^3, was taken from the SCS coating system datasheets [32]. There is some uncertainty in the elastic modulus value for Parylene C. The SCS coating system datasheet lists 2.76 GPa, which is used by many authors (e.g., [33]). However, Harder *et al.* measured a modulus between 4.1 and 5.5 GPa [34]. In this work, a middle range value of 3.8 GPa is used. The Poisson ratio of Parylene is taken to be 0.4 [33], [34].

After executing the finite element calculation, the lumped element model parameters can all be determined according to the methods of Doody *et al.* [28]. The resulting lumped-element model provides a tool for predicting the acoustic performance (center frequency, fractional bandwidth, and transmit-receive sensitivity). Fig. 4 (top) shows the predicted normalized frequency response of a single CMUT element in transmit mode. By transforming the component values across the electro-mechanical transformer, a purely electrical equivalent model can be obtained for use in SPICE circuit simulations (see the result in the middle plot of Fig. 4).

The transducer model has also been integrated into a Matlab script (The MathWorks Inc., Natick, MA) that captures the effects of acoustic cross-coupling between neighboring elements of arrays with various pitches. In the coupled simulation, each element is forced not only by the electrostatic force arising from the applied drive voltage, but also by the pressures generated by the motion of all other elements in the array. This leads to a matrix computation, with a fully populated transfer function matrix including the phase lag and geometric spreading of the transmitted pressure field for each individual element. The unknowns to be computed are the volume velocities of the elements in the array, U_m, which are

TABLE III. MATERIAL PROPERTIES AND LAYER THICKNESSES USED IN THE COMPUTATIONAL MODEL.

Material	Young's modulus (GPa)	Poisson's ratio	Density (kg/m^3)	Layer thickness (nm)
Oxide	74.6	0.20	2200	920
Aluminum	71.8	0.33	2700	1060
Overglass	54.2	0.20	2250	490
Nitride cap	172.5	0.31	3100	690
Parylene C	3.8	0.40	1289	3000

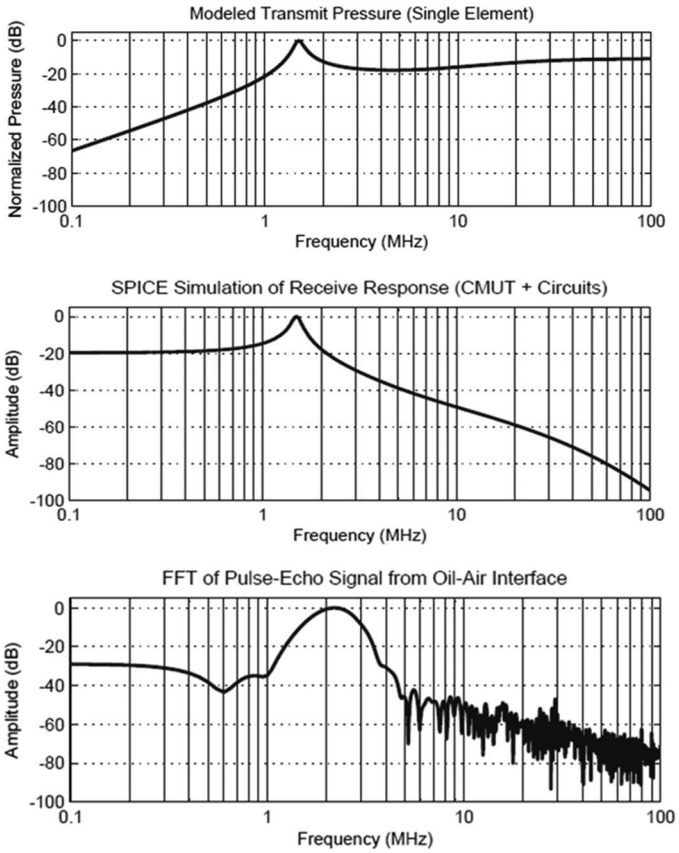

Fig. 4. (top) Single CMUT transmit frequency response predicted by lumped element model; (middle) receive response for single CMUT together with on-chip readout circuits, predicted by SPICE simulations incorporating lumped-element receive model; (bottom) experimental result from FFT of pulse-echo signal off an oil-air interface for a 4 × 8 cluster transmitting and a single CMUT receiving. (Note that because the experimental result is from a cluster, a shift in center frequency and bandwidth is observed compared with the single element simulation. This is correctly handled by the fully coupled model used for Fig. 5.)

$$U_m = H_1 V_{ac} + \sum_{n=1}^{\text{elements}} [H_2 P_{mn}(1-\delta_{mn})],$$

where δ_{mn} is the Kronecker delta function; H_1 is the transfer function computed from the lumped element transducer model, which gives the volume velocity of a single element in response to an ac voltage; H_2 is the transfer function, which gives the volume velocity of a single element in response to an external pressure presented at the element surface; and P_{mn} is the pressure field produced by the nth element at the mth element's centerpoint. P_{mn} must be computed using the Rayleigh integral, as it is in the nearfield of the transmitting element. The Rayleigh integral allows the nearfield pressure at the center of the mth element to be computed by integrating the normal surface velocity of the nth element,

$$P_{mn} = j\rho f \int_0^{2\pi}\int_0^{a} u_n(r)\frac{e^{-jkR_s(r,\theta)}}{R_s(r,\theta)} r\,\mathrm{d}r\,\mathrm{d}\theta,$$

where the surface velocity of the nth element is taken to be the static bending shape of a clamped circular plate,

$$u_n(r) = \frac{3U_{\text{dia},n}}{\pi a^2}(1-(r/a)^2)^2,$$

which involves the volume velocity of the nth element, $\mathrm{U}_{\text{dia},n}$. $\mathrm{U}_{\text{dia},n}$ is unknown initially and its presence in this expression is what leads to the full matrix problem. The distance between the surface element and the center of the mth array element is

$$R_s(r,\theta) = \sqrt{(x_n + r\cos\theta - x_m)^2 + (y_n + r\sin\theta - y_m)^2},$$

where (x_n, y_n) and (x_m, y_m) are the locations of the center of the nth and mth elements in the planar array. The Rayleigh integral can be computed numerically at each frequency and for each element in the matrix to produce the operator Ξ_{mn},

$$\Xi_{mn} = \frac{P_{mn}}{U_{\text{dia},n}} = j\rho f \int_0^{2\pi}\int_0^{a} \frac{3}{\pi a^2}(1-(r/a)^2)^2 \frac{e^{-jkR_s(r,\theta)}}{R_s(r,\theta)} r\,\mathrm{d}r\,\mathrm{d}\theta;$$

this leads to the linear algebraic problem that must be solved to find the unknown volume velocities,

$$U_m = H_1 V_{\text{ac}} + \sum_{n=1}^{\text{elements}} [H_2 \Xi_{mn} U_n (1-\delta_{mn})],$$

which can be expressed in matrix form as

$$\begin{bmatrix} 1 & -H_2\Xi_{12} & \cdots & -H_2\Xi_{1\text{n}} \\ -H_2\Xi_{21} & 1 & \cdots & -H_2\Xi_{2\text{n}} \\ \vdots & \vdots & \ddots & \vdots \\ -H_2\Xi_{\text{m1}} & -H_2\Xi_{\text{m2}} & \cdots & 1 \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_{\text{n}} \end{bmatrix} = \begin{bmatrix} H_1 V_{\text{ac}} \\ H_1 V_{\text{ac}} \\ \vdots \\ H_1 V_{\text{ac}} \end{bmatrix}.$$

At any given frequency, the matrix can be inverted numerically to compute the volume velocities of each element in the array. Once the volume velocities are known, the transmitted pressure at any point in the field can be computed using the Rayleigh integral. This computation is also valid in the nearfield at the surface of the array, allowing array surface pressures to be computed.

An example result is shown in Fig. 5 for a 4 × 8 cluster of CMUTs driven by a 100 V dc bias plus a 75 V (peak) continuous wave ac drive signal. This is a fully coupled simulation and shows the transmitted field pressure at a distance of 11 mm on the center axis of the array. The simulation predicts a 2.06 MHz center frequency and a half-power fractional bandwidth of 76% in the field, which closely agrees with experimental results (see Section III-B). Fig. 5 also shows the diffraction loss from the highest pressure point on the surface of the array to the field point. At 2.06 MHz, the diffraction loss is predicted to be

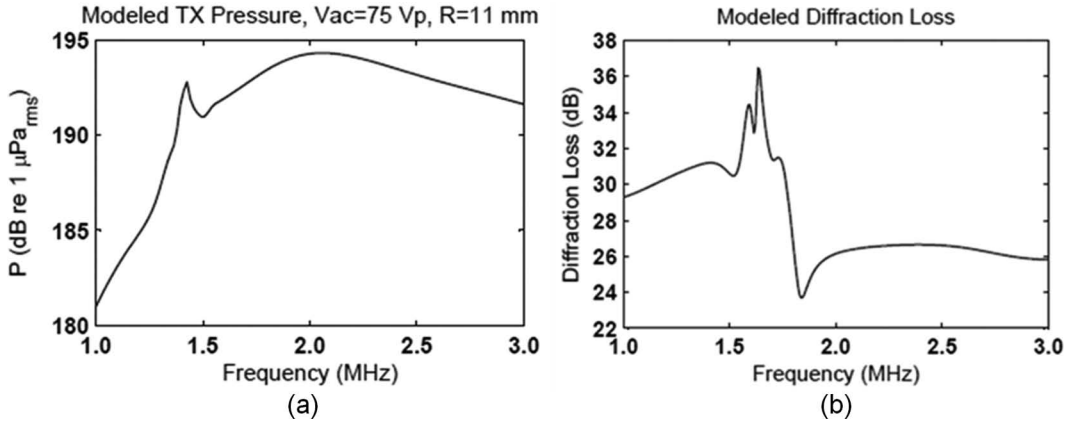

Fig. 5. Simulated transmitted pressure for a 4 × 8 array of CMUTs transmitting into a water tank. The elements are driven with a 100 V dc bias and a 75 V ac drive. (a) The pressure at a point in the field 11 mm axially out from the center of the array and (b) the diffraction loss from the highest pressure location at the surface of the array to the field point at 11 mm on axis.

26 dB. As discussed in Section III-B, this result can be used to estimate the surface pressure based on experimental field pressure measurements.

C. Array and On-Chip Circuit Design

The 2-D array design is composed of repeatable 4 × 4 element CMUT/circuit blocks tiled together to form the full 32 × 32 grid. Individual elements are arranged on a hexagonal grid, with centers equally spaced 250 μm from neighbors to accommodate half-wavelength pitch. As shown in the left photograph in Fig. 6, the CMUTs, CMOS circuitry, and routing lines are located side by side within the confines of the grid. The full 9.7 × 9.4 mm array chip is pictured on the right in Fig. 6, showing the 8 × 8 tiled arrangement of the 16-element blocks. The CMUT/circuit blocks are designed with a layout that maps output signals onto repeated groups of parallel output bus lines running to bonding pads around the chip perimeter. The routing capacity is sufficient to accommodate up to 1,024 multiplexed receive signals, which is enough for a full 128 × 128 array. On transmit, the array is designed to be driven by off-chip pulser circuits. Transmit bus lines are routed to 128 clusters of 2 × 4 elements each. These elements can be grouped at the system level into larger blocks customized for a given transmit beamforming strategy (e.g., synthetic aperture, flash, etc. [35]–[37]). Eventually, for more beamforming flexibility, a high-voltage CMOS process could be used to produce an array with individual elements driven by on-chip pulsers [20], [38]–[40].

Fig. 7 shows a block diagram of the circuit path seen by each CMUT. Each element is paired with a buffer to reduce its electrical output impedance and to drive the subsequent circuit stages. A multiplexer combines the signals from 16 neighboring elements onto a single output line, and a pad buffer drives the output signal to the chip perimeter and across a micro coaxial cable to the imager. In addition, each element buffer is protected by an active switch that creates a low-impedance path from the input node to the power supply rail during every transmit event, ensuring that high-voltage pulses applied to CMUT lower electrodes do not cause the input voltage of the buffer to rise to a damaging level. When the switch is open, its large "off" resistance serves to convert the CMUT output current to a voltage. Fig. 8 shows a transistor-level schematic of the receive signal chain for a single CMUT, including the buffer, the multiplexer channel, and the pad buffer. For SPICE simulations, this schematic was integrated with an electrical equivalent of the lumped-element CMUT model from Fig. 2. As shown in Fig. 4 (middle), simulations predict that the buffer has sufficient bandwidth to cover the frequency range of the CMUT. Because it is difficult to test the circuit alone under conditions that replicate the CMUT loading of the circuit input node, the SPICE simulation results have been compared with test results obtained from the CMUT buffer output during acoustic testing in the water tank [see Fig. 4 (bottom)]. Experimental details are described in Section III-B below.

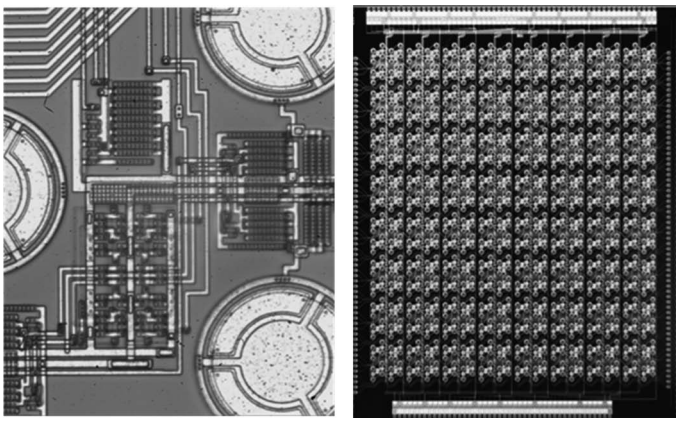

Fig. 6. (left) Photograph of CMUT elements with on-chip buffering and multiplexing circuitry. As shown, the readout circuits are located just adjacent to the elements; to improve fill factor the circuits and routing lines could be located directly below elements by using a CMOS process with more metal layers. (right) Photograph of full 32 × 32 array (9.7 × 9.4 mm). The visible rectangular grid pattern indicates the arrangement of 4 × 4 clusters of elements that are multiplexed to share a physical output line.

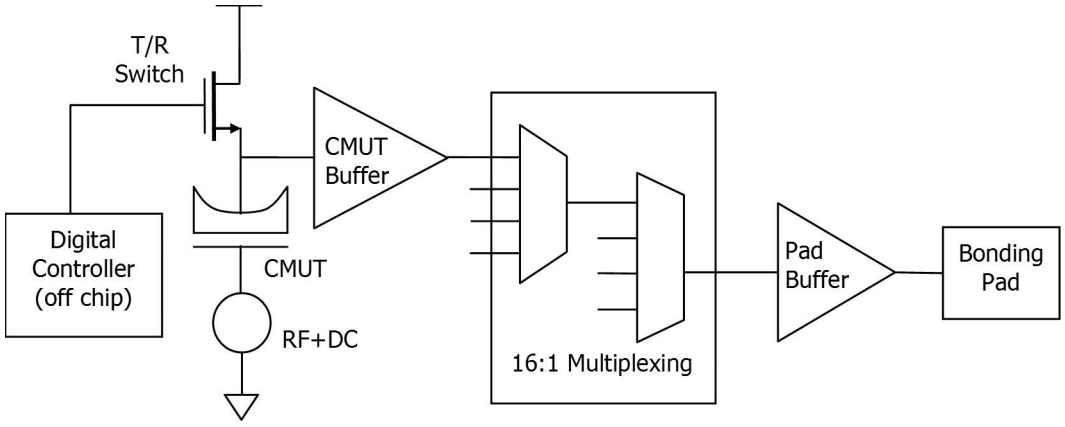

Fig. 7. Block diagram of the signal chain seen by each element. The dc bias and RF transmit pulses are applied to the bottom plate of each CMUT. A transmit/receive (T/R) switch protects the input of the CMOS electronics in the on position and converts the CMUT output current to a voltage in the off position. All elements are first buffered and then multiplexed in groups of 16. A pad buffer drives the bonding pad and cable impedances.

The analog circuits included in the current design show proof-of-concept for integrating signal processing electronics on the same chip as the ultrasound array. In future designs, additional analog circuits such as variable-gain amplifiers and filters could be incorporated to increase the dynamic range and reduce system cost and complexity. With more advanced CMOS processes, it could become feasible to integrate the full receive chain including ADCs directly on the array substrate [41].

D. Array Fabrication

The CMUT-in-CMOS fabrication process is illustrated in Fig. 9. The critical CMUT and circuit layers are deposited and patterned as part of a standard foundry CMOS process, in this case the ON Semiconductor ABN 1.5 μm n-well process (ON Semiconductor, Phoenix, AZ; formerly AMI Semiconductor), which provides two metal and two polysilicon layers. Prototyping with this process was accomplished using a multi-user fabrication run provided through the MOSIS service at the University of Southern California. As shown, the geometry of the metal layers and dielectric openings is designed to provide the CMUT structural components as well as the sacrificial layer and etch port access needed to create the CMUT gap. For the 32×32 array presented here, chips arrived from the foundry as singulated dice. To protect bonding pads during the sacrificial etch, a bead of negative photoresist (Futurrex NR4-8000P, Futurrex Inc., Franklin, NJ) was manually applied around the chip perimeter and cured on a 150°C hotplate for 2 min. Screen printing or noncritical photo patterning of resist could be used for volume production. The sacrificial aluminum layer was then removed using a proprietary wet-etch solution. This etch step can also be accomplished with a standard microelectronic metal etchant such as Aluminum Etchant–Type A (Transene Inc., Danvers, MA), although etching will take 6 to 8 h, which may challenge the integrity of the photo-

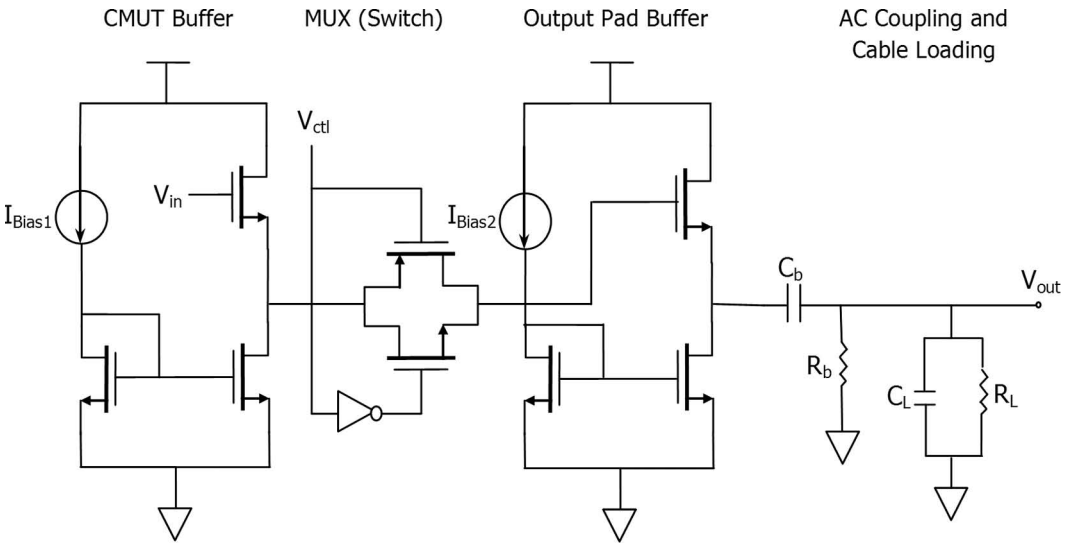

Fig. 8. Transistor-level diagram of readout circuit for every element. The CMUT elements are buffered by a simple single-stage buffer, multiplexed with pass-gate switches, and buffered by a second two-transistor buffer. Also shown are the blocking capacitor and bias resistor for ac-coupling the output to the load.

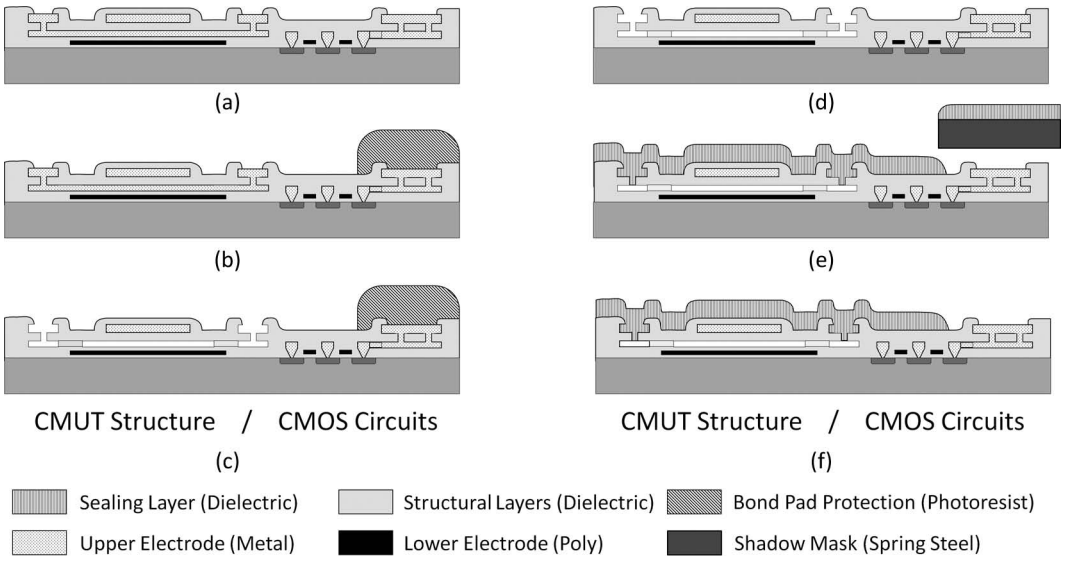

Fig. 9. Illustration of the CMUT-in-CMOS fabrication process flow. (A) Silicon die with layers patterned in CMOS foundry process; (B) photoresist is manually applied (or screen printed) around the perimeter to protect bonding pads; (C) the CMUT gap is formed by sacrificial wet etching of the lower metal layer; (D) the photoresist is stripped, and the chip is soaked in acetone/methanol and allowed to air dry; (E) dielectric is deposited to seal the CMUT cavity, and bonding pads are shadow masked to prevent coverage; (F) the completed device is ready for packaging.

resist protecting the bonding pads. Because the CMUT gap is relatively large, devices can air dry without stiction after soaking in acetone and methanol. Finally, the CMUT cavities are sealed at vacuum to prevent entry of water or contaminants into the gap. This sealing step has been accomplished by depositing Parylene-C at room temperature, or alternatively by depositing PECVD oxide, nitride, or oxynitride at 200 to 400°C. For Parylene deposition, the chip is wire-bonded to a carrier/connector before deposition, but for PECVD, a clamped shadow mask is used to keep bonding pads clear for subsequent wire bonding. Sealing of the 1.5-μm square etch holes is verified visually using an optical inspection microscope to observe the device cavities when a drop of methanol is applied to the surface. Prior to sealing, the methanol can be observed entering the cavities and retreating as surface tension and evaporation eliminate the fluid from beneath the transparent CMUT diaphragms. When a layer sufficiently thick for sealing (typically 2 to 3 μm) is deposited, the methanol no longer enters the cavities. The thickness of the Parylene layer is controlled by the mass of Parylene dimer loaded into the deposition tool, and the final thickness can be measured using a surface profilometer.

E. System Integration

After fabrication, each array chip is mounted and wire-bonded to a printed-circuit daughterboard (5 × 2 in.; 12.7 × 5.08 cm) with edge-card connections. To electrically insulate the bonding wires on the daughterboard for water tank testing, medical grade epoxy (Epo-tek 353ND/NDT, Epoxy Technology, Billerica, MA) is manually applied to the bonding region around the chip perimeter, with care taken to avoid covering the CMUTs in the central region of the chip. The daughterboard interfaces to a motherboard that provides access to array output signals, administers multiplexer addresses and trigger signals (via an on-board complex programmable logic device (CPLD) chip), and controls the transmit and dc bias configurations. The motherboard also provides an interface to a standard transducer cable that leads to a compact convertible ultrasound system with research platform software that provides access to *IQ* data (Zonare z.one, Zonare Medical Systems, Mountain View, CA). For initial water tank testing, the form factor of the interface boards was designed for ease of signal monitoring and for maximum configurability. To move toward more conventional imaging demonstrations, arrays have also been mounted on flexible circuits and incorporated into a custom probe handle manufactured using a rapid prototyping machine. This probe, shown in Fig. 10, contains the hardware necessary to interface the array to the Zonare system to collect data in simple imaging studies.

In addition to connecting to the Zonare system for data readout, the 32 × 32 array has been interfaced to a custom FPGA-based acquisition system. This system was implemented using off-the-shelf components for 64 channels of time-gain control (TGC) and analog-to-digital conversion (ADC) on receive, and 32 channels of phase-programmable high-voltage pulses on transmit. The single-board TGC/ADC/TX module (Fig. 11) was designed in-house and implemented using an 11 × 6 in (27.94 × 15.24 cm) 10-layer board with an impedance-controlled dielectric/interconnect stack to accommodate the high-speed low-voltage differential signaling (LVDS) outputs from the ADC chips. This board connects directly to a daughterboard that houses the CMUT array, and it is interfaced to an advanced FPGA demonstration board that deserializes the LVDS signals, stores the digitized data, and provides a programmable PC interface. This system offers improved

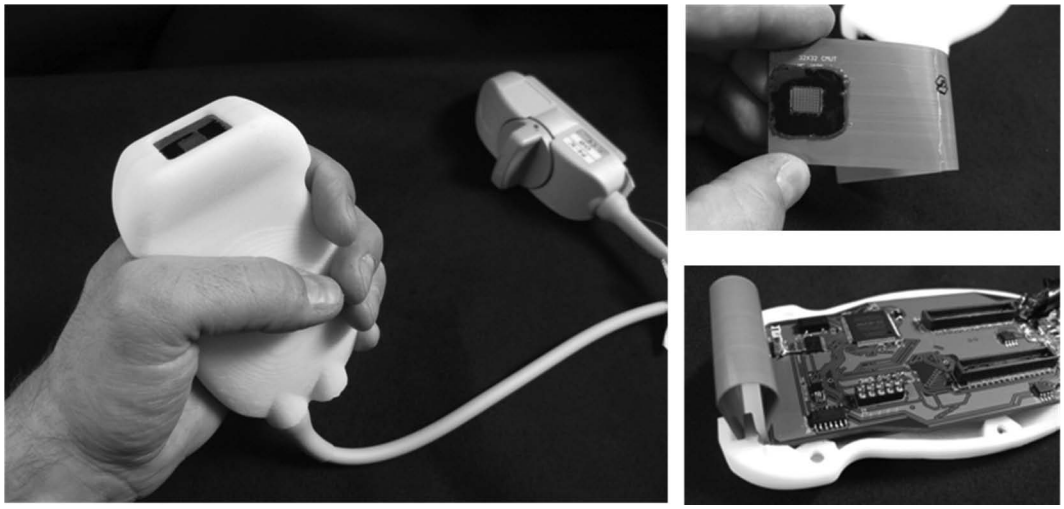

Fig. 10. (left) Photograph of the custom probe handle containing a 32 × 32 CMUT array on a flex circuit (upper right) and an electronic interface board (lower right) for connecting to the receive channels of a commercial ultrasound system. The upper right photograph shows the epoxy protection applied to the bonding wires around the perimeter of the array mounted on the flex circuit; this approach is also used on rigid PCBs for water tank testing.

control over transmit beamforming and receive data acquisition, and it provides an initial demonstration vehicle for the scale of system-level electronics needed to acquire images from the array.

For transducer characterization and phantom imaging studies, the CMUT array hardware and readout electronics were incorporated into a water tank test environment. A 50-gallon acrylic tank was filled with deionized water that was degassed, after filling, using a variant on a previous method [42]. The motherboard described above was mounted on a custom-built gimbal fixture to allow angle adjustments for the array. A six-axis robotic arm (LR-Mate 200iC, Fanuc USA, Rochester Hills, MI) was used for computer-controlled positioning of source transducers, hydrophones, and pulse-echo targets in the tank during testing. For simpler pulse-echo and imaging experiments with small targets, a small oil/water receptacle was also mounted directly on a horizontally oriented daughterboard.

III. Results

A. Fabrication Results

Release and sealing steps were successfully performed on approximately twenty 32 × 32 array chips. Fig. 12 shows SEM images of a released device before sealing, with the cross-section of both the CMUT element and the neighboring transistors visible. Visual inspection after the release etch step indicated that some yield loss initially occurred due to undesired etching of some bonding pads. The manual procedure used for covering pads was refined to include mounting each chip on a larger carrier substrate and applying the photoresist with miniature swabs under 10× magnification. This approach now yields nearly 100% pad survival on most chips.

To qualitatively evaluate the yield and uniformity of elements, each array is visually inspected before and after packaging. Typically yield loss identified in this process

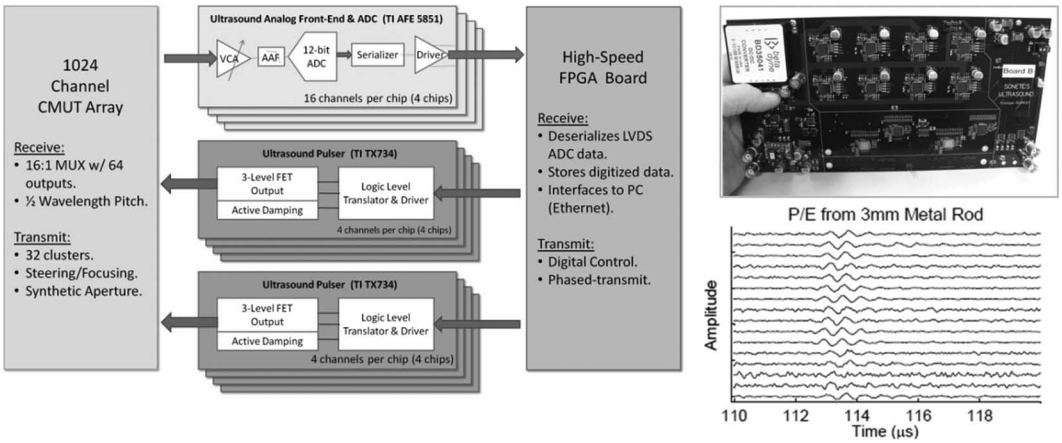

Fig. 11. (left) Block diagram of a custom system for interfacing to the Sonetics 32 × 32 CMUT array. The board processes and digitizes 64 channels of multiplexed data and provides phased transmit pulses to 32 clusters on the array. (right) Photo showing the scale of the assembled board, and pulse-echo signals (from a 3-mm metal rod in a water tank) captured using the board.

results from mishandling during the release and sealing steps (e.g., elements can be damaged by scratching the surface with tweezers while handling chips, or the shadow mask can be grossly misaligned during deposition of the PECVD dielectric sealing layer). Because yield ultimately depends on both the mechanical integrity of each element as well as electronic functionality of the on-chip readout circuit for each channel, acquisition of acoustic signals is needed to quantitatively test yield and uniformity. The testing apparatus and procedures described in Section III-B are used for this evaluation. The array is insonified uniformly with a plane wave produced by a flat source transducer placed a long distance (40 cm) from the array surface, and the Zonare imager is used to capture the signal received by every element. As shown in Fig. 13, the uniformity across the array is excellent, with the receive sensitivity of all 1024 elements within ±1.5 dB.

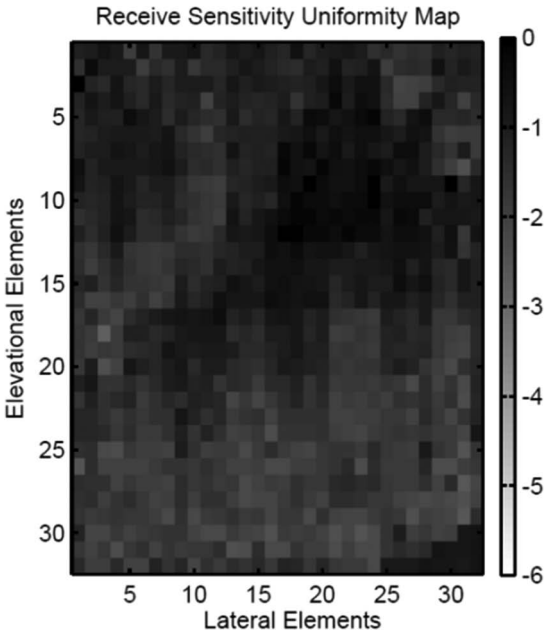

Fig. 13. Map of receive sensitivity (normalized), indicating high uniformity across the array (within ±1.5 dB) with no dead elements. Received signals from every element were captured using a Zonare commercial imaging system while the array was uniformly insonified with a 12-kPa plane wave produced by a flat 0.5-in-diameter 2.25-MHz source transducer placed 40 cm away.

B. Device Characterization

Transmit, receive, and pulse-echo performance of individual elements and clusters were evaluated using water-tank testing. The array element characterization results are summarized in Table IV. To evaluate the array's center frequency and fractional bandwidth, the pulse-echo response was measured from an oil/air interface positioned approximately 7 mm from the array surface. Elements were excited with a broadband 32-μJ pulse from a 5900PR pulser-receiver (Olympus NDT, Waltham, MA), and the received signal (Fig. 14, top) was captured using a digital oscilloscope (LeCroy Waverunner 44MXi, LeCroy Corporation, Chestnut Ridge, NY). The FFT of the pulse-echo signal (Fig. 14, bottom) was computed using Matlab, showing a 2.1 MHz center frequency and a −6-dB fractional bandwidth of approximately 57%. The bandwidth is substantially lower than many CMUTs reported in the literature [18], [20], likely due to the low element fill factor [43]–[45]. As discussed elsewhere in this paper, the fill factor can be improved dramatically by locating CMUTs directly above readout circuits using a CMOS process with more metal layers.

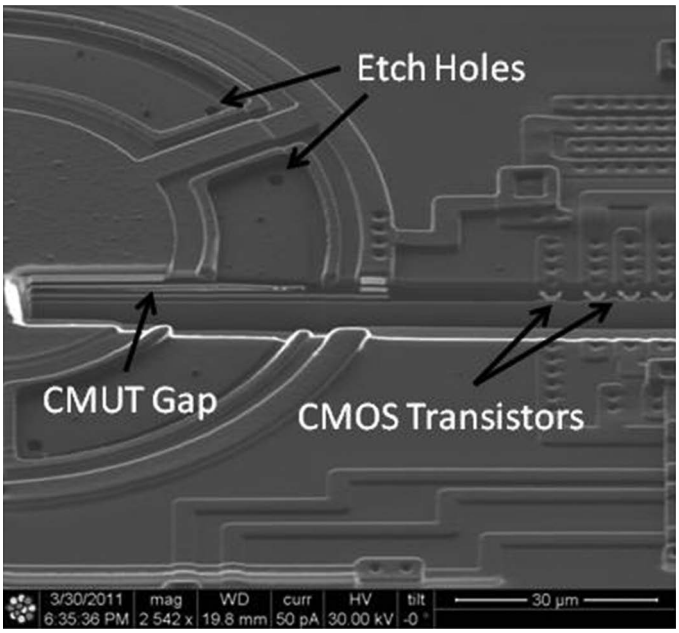

Fig. 12. Scanning electron micrograph of the CMUT after release but before sealing. The cross-section shows the CMUT layers including the upper and lower electrodes as well as the gap. The source/drain contacts and gates of CMOS transistors reside on the same layers, directly adjacent to the CMUT.

For receive sensitivity characterization, the array was biased with a dc voltage in the range of 80 to 200 V and was placed in the far field (15 cm from the face) of an unfocused 12.5-mm diameter, 2.25-MHz transducer (Panametrics A306S, Olympus NDT, Waltham, MA). An Onda HGL-0400 hydrophone (Onda Corporation, Sunnyvale, CA) was used to determine the proper drive amplitude to produce a 50-kPa 20-cycle sinusoidal burst at the center frequency ~2 MHz). The CMUT output, buffered by the on-chip receive circuit, was then captured with an oscilloscope (LeCroy WaveRunner 44Mxi). A receive sensitivity of 2.4 mV/kPa was measured under biasing conditions typical for the imaging experiments described below (<100 V dc). Results as high as 12 mV/kPa were obtained with higher dc biasing (180 V dc). To determine the noise-equivalent pressure or minimum detectable pressure, the output noise of the receive circuit with no acoustic input was measured using a spectrum analyzer (Agilent 3495A, Agilent Technologies Inc., Santa Clara, CA). The resulting noise amplitude (15.3 nV/$\sqrt{\text{Hz}}$) was divided by the receive sensitivity, yielding a typical minimum detectable pressure of 6.4 mPa/$\sqrt{\text{Hz}}$ or approximately 6.4 Pa for the

TABLE IV. ELEMENT AND ARRAY MEASUREMENT RESULTS.

Parameter	Value	Comment
Center frequency	2.1 MHz	Determined using FFT of pulse-echo signal
Fractional bandwidth	40–60%	Determined using FFT of pulse-echo signal
Receive sensitivity	2.4 mV/kPa	Measured with −100 V dc bias
Electronic noise	15.3 nV/$\sqrt{\text{Hz}}$	Measured with spectrum analyzer
Noise-equiv. pressure	6.4 mPa/$\sqrt{\text{Hz}}$	Converted from above
Transmit surface pressure	142 kPa	For elements excited by 32-μJ broadband pulse
Dynamic range	86.8 dB	Surface pressure divided by NEP
Uniformity (RX Sens.)	±1.5 dB	Measured with captured array data
Element yield	>99%	Typical >1010 out of 1024 elements

measured CMUT bandwidth. With 30× averaging, this can be improved to 1.2 Pa.

To evaluate the pressure output of the array, a hydrophone was used to measure the field pressure produced by various sized transmit clusters. As noted in Table I, the smallest transmit clusters on the chip consist of 2 × 4 elements (spaced at 250 μm pitch), which are electrically connected together. At the PCB level, mechanical switches combine these clusters into larger groups of elements such as 4 × 8, 8 × 16, or the full 32 × 32 aperture. The measured field pressure from a 4 × 8 group of elements, excited by a 32-μJ pulse (Panametrics 5900PR pulser-receiver), was 6.7 kPa at 11 mm from the array. To obtain the pressure at the surface, the measured data must be compensated for diffraction losses (no attenuation is accounted for because measurements were performed in a water tank). As indicated in Fig. 5, the model described above predicts a diffraction loss of 26.5 dB for 11 mm distance at the 2.06 MHz center frequency. Therefore, the output pressure at the surface is estimated to be 142 kPa. The dynamic range of a CMUT element can be expressed by dividing the maximum transmit surface pressure by the minimum detectable pressure [46]. Based on this method, each CMUT shows a dynamic range of approximately 87 dB over the measured bandwidth.

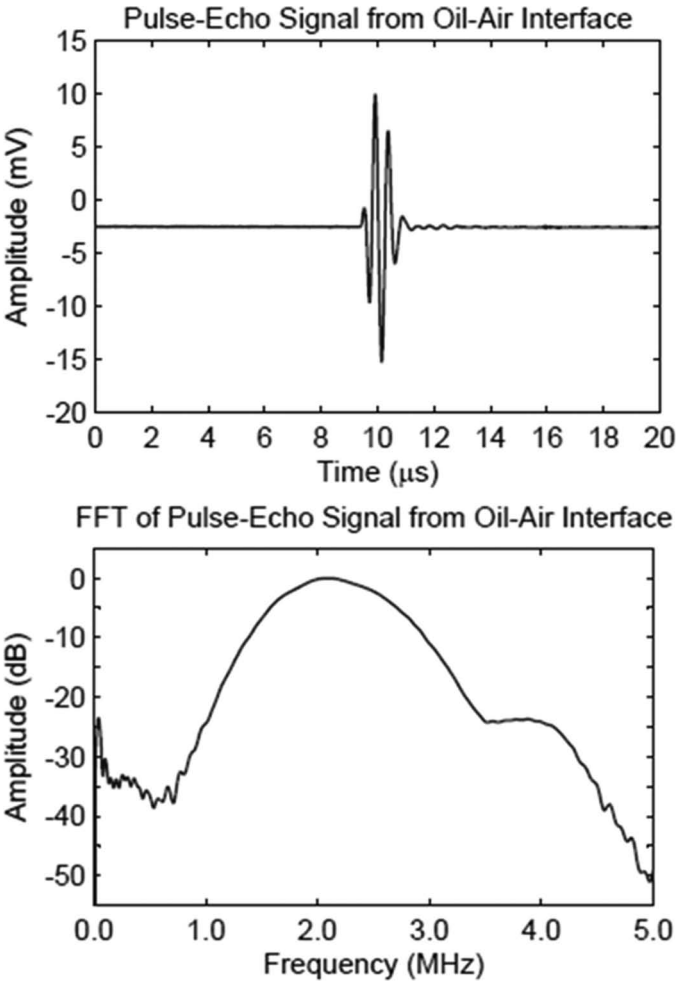

Fig. 14. (top) Time-domain pulse-echo signal captured by a single CMUT receive element in response to a full-aperture planar transmit echoing off an oil-air interface located approximately 7 mm from the array. (bottom) Fast Fourier transform of the pulse-echo signal, indicating a center frequency of 2.1 MHz with 57% bandwidth. The bandwidth can be improved in the future by increasing the array fill factor.

C. Imaging Results

The 32 × 32 array has been used to acquire 3-D image data for a variety of targets, including fishing lines, brass rods with a range of diameters, and polished flat-ended steel rods. For these initial imaging demonstrations, all elements were transmitted in phase to insonify the region of interest. Echo data from all 1024 elements were acquired using the Zonare imager for some experiments and the custom readout board (Fig. 11) described above for others. For each transmit event, the Zonare system acquires 64 *IQ* data channels in parallel, with a pulse repetition frequency of 200 Hz. Sixteen transmit firings are required to read out all 1024 CMUT elements, which are multiplexed 16:1 on the chip. Each full-array readout therefore takes 80 ms, giving a volume acquisition rate of 12.5 volumes/second. For 30× averaging of volume images, 500 to 600 frames of data are acquired, taking 2.5 s for each averaged image. The custom FPGA-based readout board provides additional flexibility in triggering and acquisition rate, so that the same 30× averaged data can be captured at 10 volumes per second (for targets <15 cm deep). Prior to assembly of the custom board, a design flaw was discovered, which resulted in data being accessible from only 32 of the 64 channels (pin assignments on one connector leading to the FPGA board were erroneous). This meant that only 512 of the 1024 CMUTs were accessible with the custom board. Therefore, most imaging experiments were

conducted using the Zonare system which was capable of full 64-channel readout. *IQ* data were downloaded to a PC (via USB stick for the Zonare system or ethernet for the custom board), and data were sorted, converted to RF, and analyzed in Matlab. An example of RF waveforms captured with the custom board is shown in Fig. 11. Image reconstruction was performed in Matlab using a synthetic aperture approach that accomplishes dynamic receive focusing at every voxel. Specifically, waveform reconstruction for each voxel was computed using a delay and sum algorithm that accounted for transmit and receive path lengths to and from all transmit and receive voxels. Using this approach, full resolution 3-D volumes were reconstructed.

For imaging experiments, targets were placed in the near field of the 9 × 7 mm aperture, meaning that the imaging depth was limited to approximately 3 to 5 cm. Fig. 15 shows a reconstructed slice image of four 0.15-mm nylon fishing lines suspended in a water tank, perpendicular to the elevational axis of the array. The lateral and axial profiles of the lines are shown in the lower plots in Fig. 15. These coincide with the beam profiles of the array because the scatterers are small compared with a wavelength. The −6-dB axial beam width measures approximately 1.2 mm, which is consistent with expectations based on the 2.1 MHz center frequency and 57% bandwidth. The lateral beam profile reveals side lobes 15 dB lower than the main lobe. As shown, these can be suppressed by applying a 2-D Hanning window apodization to the receive data before reconstruction. Fig. 16 shows a 3-D image of the fishing lines, displayed using OsiriX, an open-source medical image viewing software [47].

IV. Conclusion

This work demonstrates the feasibility of integrating thousands of ultrasound transducer elements together with CMOS electronics on a single chip using a high-volume integrated circuit manufacturing process with minimal added complexity. To the authors' knowledge, this is the first demonstration of using a CMOS fabrication process to produce a planar ultrasound array capable of capturing 3-D image data. The 32 × 32 array was designed using repeatable transducer/circuit/routing blocks, which provide the capacity to scale up to a fully-populated 128 × 128 element array. Array chips have been produced with more than 99% working elements (100% on some arrays) and only approximately ±1.5 dB sensitivity variations between elements. On-chip CMOS multiplexers reduce the signals from 1024 elements to 64 physical outputs. Data from rudimentary imaging experiments have been collected by interfacing the CMUT array to both a commercial imager and a custom FPGA-based transmit/receive board. The results provide a practical demonstration of the CMUT-in-CMOS approach, showing that a foundry CMOS process with only minor augmentation can produce integrated imaging arrays. Further development of this technology will focus on improving element bandwidth and sensitivity while maintaining the cost and reliability advantages of using CMOS manufacturing. This sets the stage for diagnostic ultrasound systems with increased levels of integration, leveraging the cost and performance advantages of system-on-chip integration even within the imaging array.

Acknowledgments

The authors are grateful to T. Penird, T. Glenn, and A. Dubuc for rapid prototyping and test fixture machining, Dr. C. Yang for circuit design contributions, and D. Sanzi for manuscript assistance. Also, the authors thank N. Sancimino and V. Marques (Texas Instruments) for design guidance and access to electronic components. This work

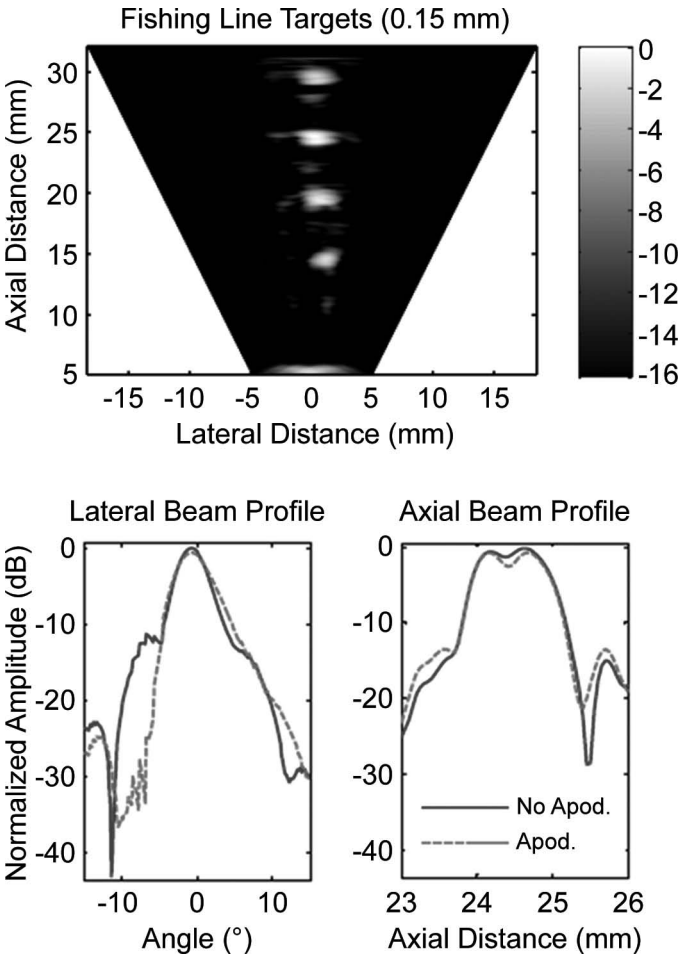

Fig. 15. (top) Axial-lateral slice image of four 150-μm fishing lines suspended in a water tank, reconstructed from a 3-D data set captured using the Zonare z.one scan engine with 30 frames averaged. (bottom left) Lateral beam profile obtained with an angular slice through the third line target, located 24 mm from the array. The side lobes, which are visible at −15 dB, are reduced by applying a Hanning window apodization to the receive aperture, as shown in the dashed trace. (bottom right) Axial beam profile obtained by an axial cut across the third line target. The −6-dB beam width measures 1.2 mm, which is consistent with the 2.1 MHz, 57% bandwidth of the elements.

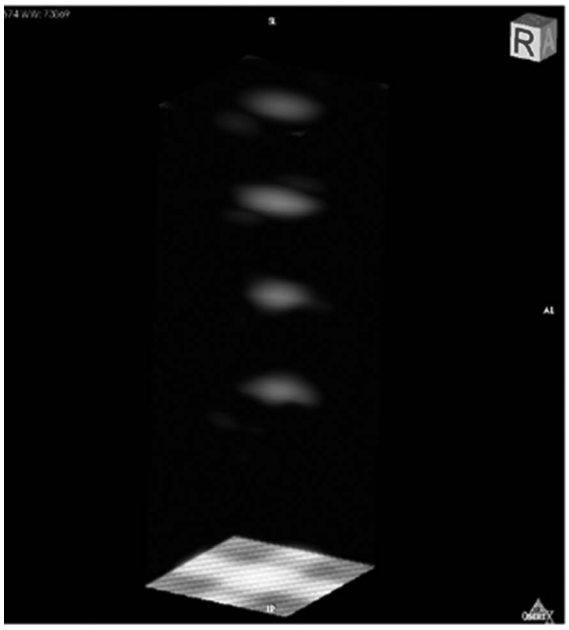

Fig. 16. Three-dimensional image of four 150-μm-diameter nylon fishing lines. The array location is shown to aid in visualizing the lines. The image is displayed with a 16-dB dynamic range. The extent of the lines appears limited because of specular reflections and the limited aperture size of the array.

was supported by the NSF SBIR/STTR Program under Award No. 0450493. Device processing was performed in the Lurie Nanofabrication Facility (Ann Arbor, MI), a member of the National Nanotechnology Infrastructure Network.

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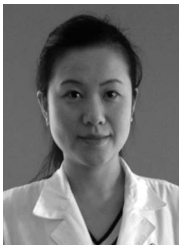

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