

# Mark D. Hempstead

## Associate Professor

Department of Electrical and Computer Engineering

Tufts University

Medford, MA 02155

Email: [mark@ece.tufts.edu](mailto:mark@ece.tufts.edu)

Personal Website: <https://sites.tufts.edu/tcal/people/prof-hempstead/>

(Updated Feb 11<sup>h</sup>, 2019)

## Brief Description of Research Interests

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Mark Hempstead is an Associate Professor in the Department of Electrical and Computer Engineering at Tufts University. His research group, the Tufts Computer Architecture Lab, investigates methods to increase energy efficiency across the boundaries of circuits, architecture, and systems. His research has been applied to a range of platforms from embedded systems, IoT, chip multiprocessors, and high performance computing. Currently, they are exploring the performance and energy benefits of heterogeneity in future many-accelerator architectures; the security implications of the thermal-side channel; methods to automatically generate shared hardware accelerators from source code; power-aware hardware and software for Android devices, and flexible workload characterization tools. His group has published in several different research communities including high performance computer architecture, embedded systems, workload characterization, mobile-systems, and Internet-of-Things (IoT).

## EDUCATION

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**PhD**, Engineering Sciences, June 2009,

**Harvard University**, Cambridge MA

*Academic Advisors:* Prof. Gu-Yeon Wei and Prof. David Brooks (Co-Advised)

*Dissertation:* "Accelerator-Based Architectures for Wireless Sensor Network Applications"

*Dissertation Committee:* Prof. Gu-Yeon Wei, Prof. David Brooks, Prof. Margo Seltzer

**S.M** Engineering Sciences, June 2005

**Harvard University**, Cambridge MA

**B.S.** Computer Engineering, Summa Cum Laude, May 2003

**Tufts University**, Medford MA

## HONORS, AWARDS AND MEMBERSHIPS

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2014 Drexel University Allen Rothwarf Award for Teaching Excellence

2014 Drexel College of Engineering Excellence in Research Award

2014 NSF CAREER Award

2012 HPCA Best Paper Nominee

2006 SRC Design Contest Winner

2002- Member Eta Kappa Nu Electrical Engineering Honor Society

2002- Member Tau Beta Pi Engineering Honor Society

**Memberships:** IEEE, ACM, IEEE Computer Society, ACM SIGARCH

## WORK EXPERIENCE

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**Tufts University, Medford MA Associate Professor, Electrical and Computer Eng.** 9/2015 – present  
**Tufts University, Medford MA Adjunct Associate Professor, Computer Science** 9/2015 – present  
 Director of the Tufts Computer Architecture Lab.  
 Founding Director of the Tufts Masters Degree Program in Computer Engineering

**Drexel University, Philadelphia PA Associate Professor (with Tenure)** 5/2015 – 8/2015

**Drexel University, Philadelphia PA Junior Colehower Chair Assistant Professor** 1/2010 – 5/2015  
 Developed a research program in power-aware computer architecture, low power circuit design, and power-aware systems. Research topics include energy-efficient microarchitecture, accelerator-based architectures, workload characterization, and power-agile computing. Re-imagined the both the undergraduate and graduate computer architecture sequences to include multi-core processing and power-aware. Winner of University wide teaching award and NSF CAREER award. Advisor to ten graduate students: 8 PhD and 2 MS.

**ARM Ltd., Cambridge UK Research Intern, PostDoc, R&D** 7/2009 – 11/2009

**Harvard University, Cambridge MA Research Assistant** 9/2003 – 6/2009

**Intel Corporation, Hudson MA Research Intern, VSSAD Group** 5/2005 – 8/2005

## TEACHING EXPERIENCE

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**Tufts University Associate Professor**  
 EE 126 Computer Engineering (Computer Architecture) Fall 2015, Fall 2016, Fall 2017  
 EE 156/COMP 140 Advanced Computer Architecture Spring 2016, Spring 2018, Spring 2019  
 EE 193/COMP 150 Introduction to Internet of Things Fall 2016

### At Drexel as Course Designer and Course Lead:

ECEC-414 High Performance Computing (UG) Winter 2014, Spring 2012  
 ECEC-412 Modern Processor Design (UG) Winter'15, Fall'13, Spring'13, W'12  
 ECEC-623 Adv. Parallel Computer Architecture (Grad) Spring 2015, Sp'14, W'13, Sp'11  
 ECEC-622 Parallel Computer Architecture (Grad) Winter 2011, Spring 2010  
 ECEC-621 High Performance Computer Architecture (Grad) Winter'15, W'14, F'12, F'10, W '10  
 ECEC-690 Advanced Programming C/C++(Grad) Fall 2014

### At Drexel as Recitation Instructor:

ENGR-232 Dynamic Engineering Systems Winter 2012  
 ECE-200 Digital Logic Design Spring'15, Sp'14, F'13, Sp'12, F'11

**Tufts University Lecturer**  
 EE26 Digital logic systems Spring 2009

**Resident Tutor, Lowell House Harvard University – (9/2006 – 6/2009)** Lived in an undergraduate residence. Responsible for the resident life of 35 undergraduates. Responsibilities also include academic advising.

## ARCHIVAL PEER-REVIEWED JOURNAL, CONFERENCE PUBLICATIONS

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**Quantifying Process Variations and Its Impacts on Smartphones.** Guru Prasad Srinivasa, Scott Haseley, Mark Hempstead, Geoffrey Challen. *The International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2019

**Machine Learning on the Thermal Side-Channel: Analysis of Accelerator-rich Architectures.** David Werner, Kyle Juretus, Ioannis Savidis and Mark Hempstead. *The 36th IEEE International Conference on Computer Design (ICCD)*, Oct 2018.

**Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces.** Michael Lui, Karthik Sangaiah, Mark Hemsptead, Baris Taskin. *The International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2018.

**SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation of CMP and HPC Workloads.** K. Sangaiah, M. Lui, R. Jagtap, S. Diestelhorst, S. Nilakantan, A. More, B. Taskin, and M. Hempstead. *ACM Transactions on Architecture and Code Optimization (TACO)*, March 2018.

**Algorithms for CPU and DRAM DVFS Under Inefficiency Constraints.** Rizwana Begum, Guru Prasad Srinivasa, Geoffrey Challen, and Mark Hempstead. *The 34th IEEE International Conference on Computer Design (ICCD)*, Oct 2016.

**Uncore RPD: Rapid Design Space Exploration of the Uncore via Regression Modeling.** Karthik Sangaiah, Mike Liu, Siddharth Nilakantan, Baris Taskin, Mark Hempstead. *In the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. Oct 2015.

**Power Agility Metrics: Measuring Dynamic Characteristics of Energy Proportionality.** Rizwana Begum and Mark Hempstead. *In the International Conference on Computer Design (ICCD)*. Oct 2015.

**Combative Cache Efficacy Techniques: Analysis of cache replacement in the context of independent prefetching in last level cache.** Cesar Gomes and Mark Hempstead. *In the International Conference on Computer Design (ICCD)*. Oct 2015.

**Energy-Performance Trade-offs on Energy-Constrained Devices with Multi-Component DVFS.** Rizwana Begum, Guru Prasad Srinivasa, Mark Hempstead and Geoffrey Challen. *In the IEEE International Symposium on Workload Characterization (IISWC)*, Oct 2015.

**SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation.** Siddharth Nilakantan, Karthik Sangaiah, Ankit More, Giordano Salvador, Baris Taskin, Mark Hempstead, *In the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March. 2015.

**Effects of Non-determinism in Hardware and Software Simulation with Thread Mapping.** Giordano Salvador, Siddharth Nilakantan, Ankit More, Baris Taskin, M. Hempstead, *28th International Conference on VLSI Design and 14th International Conference on Embedded System Design 2015 (VLSID ES)*, Jan. 2015.

**Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation.** Siddharth Nilakantan, Scott Lerner, M. Hempstead, Baris Taskin. *28th International Conference on VLSI Design and 14th International Conference on Embedded System Design 2015 (VLSID ES)*, Jan. 2015.

**Static Thread Mapping for NoC CMPs via Binary Instrumentation Traces.** Giordano Salvador, Siddharth Nilakantan, Ankit More, Baris Taskin, M. Hempstead. *32nd IEEE International Conference on Computer Design 2014 (ICCD)*, Oct. 2014.

**Epoch Profiles: Microarchitecture-Independent Application Analysis and Microarchitectural Optimization.** Trevor E. Carlson, Siddharth Nilakantan, M. Hempstead, Wim Heirman. *IEEE Computer Architecture Letters (CAL)*, Jan-July 2014.

**Register Allocation and VDD-gating algorithms for Out-of-Order Architectures.** Steven Battle, and Mark Hempstead. *International Conference on Computer Design (ICCD)*. Oct 2013. **(acceptance rate: 25%)**

**Characterizing the Costs and Benefits of Hardware Parallellism in Accelerator Cores.** Steven Battle, and Mark Hempstead. *International Conference on Computer Design (ICCD)*. Oct 2013. **(acceptance rate: 25%)**

**Platform-independent characterization of function-level communication in workloads using Dynamic Binary Instrumentation.** Siddharth Nilakantan, Mark Hempstead. *In 2013 IEEE International Symposium on Workload Characterization (IISWC)*. Sept 2013. **(acceptance rate: 30%; citations 2)**

**Metrics for Early-Stage Modeling of Many-Accelerator Architectures.** Siddharth Nilakantan, Steven Battle, and Mark Hempstead. *Computer Architecture Letters (CAL)*, 2012. **(acceptance rate: 24%; citations 3)**

**Flexible Register Management using Reference Counting.** Steven Battle, Andrew Hilton, Mark Hempstead, Amir Roth. *International Symposium on High Performance Computer Architecture (HPCA)* . Feb 2012 **(acceptance rate: 17%, citations: 2) [Best Paper Nominee]**

**The Accelerator Store Framework for High-Performance, Low-Power Accelerator-based Systems** Mike Lyons, Mark Hempstead, David Brooks, Gu-Yeon Wei. *ACM Transactions on Architecture and Code Optimization (TACO)*. Also Invited Presentation at HiPEAC, Paris France. January, 2012. **(citations: 20)**

**Evaluation of an Accelerator Architecture for Speckle Reducing Anisotropic Diffusion.** Siddharth Nilakantan, Srikanth Annangi, Nikhil Gulati, Karthik Sangaiah and Mark Hempstead. *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*. Taipei, Taiwan, October 2011. **(acceptance rate: 38%, citations 3)**

**An Accelerator-Based Wireless Sensor Network Processor in 130 nm CMOS.** Mark Hempstead, Gu-Yeon Wei, and David Brooks. *IEEE Transactions on Emerging and Selected Topics in Circuits and Systems (JETCAS)*. Vol. 1, Num 2. June 2011 **(citations: 17)**

**The Accelerator Store framework for high-performance, low-power accelerator-based systems.** Michael Lyons, Mark Hempstead, Gu-Yeon Wei, and David Brooks. *Computer Architecture Letters (CAL)* Nov 2010. **(acceptance rate: 24%, citations: 18)**

**Architecture and Circuit Techniques for Low-Throughput, Energy-Constrained Systems Across Technology Generations,** Mark Hempstead, Gu-Yeon Wei and David Brooks. *In Proceedings of the International Conference On Compilers, Architecture, And Synthesis For Embedded Systems (CASES)*. Seoul South Korea. October 2006. **(acceptance rate: 41%, citations: 22)**

**A Realistic Power Consumption Model for Wireless Sensor Network Devices,** Qin Wang, Mark Hempstead, and Woodward Yang. *In Proceedings of the Third Annual IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON)*. Reston, VA, September 2006. **(acceptance rate: 26%, citations: 276)**

**Power and Thermal Effects of SRAM vs. Latch-Mux Design Styles and Clock Gating Choices.** Yingmin Li, Mark Hempstead, Patrick Mauro, David Brooks, Zhigang Hu, Kevin Skadron. *In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'05)*, San Diego, CA, August 2005 **(acceptance rate: 23%, citations: 9)**

**An Ultra Low Power System Architecture for Wireless Sensor Network Applications**, Mark Hempstead, Nikhil Tripathi, Patrick Mauro, Gu-Yeon Wei, and David Brooks *In Proceedings of the 32<sup>nd</sup> International Symposium on Computer Architecture (ISCA)*, Madison, WI, June 2005. (**acceptance rate: 23%, citations: 155**)

**Simulating the Power Consumption of Large-Scale Sensor Network Applications**, Victor Shnayder, Mark Hempstead, Bor-rong Chen, Geoff Werner-Allen, and Matt Welsh. *In Proceedings of the Second ACM Conference on Embedded Networked Sensor Systems (SenSys'04)*, Baltimore, MD, November 2004 (**acceptance rate: 14%, citations: 1063**)

#### **INVITED AND WORKSHOP PUBLICATIONS (PEER-REVIEWED)**

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**Fingerprinting Coarse-Grained Reconfigurable Accelerators Using Data Movement and Structural Similarities in Applications**, P. Mokri and M. Hempstead, *Boston Area Computer Architecture (BARC) Workshop*, January 2018.

**Cache Block Watermarking: Over-engineered and Underwhelming**, Cesar Gomes, Steven Battle, Siddarth Nilakantan, and Mark Hempstead. In proceedings of the Workshop on Negative Outcomes, Post-mortems, and Experiences (NOPE) at MICRO, October 2017.

**Separated by Birth: Hidden Differences Between Seemingly-Identical Smartphone CPUs**, Guru Prasad Srinivasa, Rizwana Begum, Scott Haseley, Mark Hempstead, and Geoffrey Challen. *In Proceedings of the 18th Workshop on Hot Topics in Mobile Computing Systems and Applications (HotMobile'17)*

**ReconfASTs: Early-stage Identification of Reconfigurable Accelerators with Annotated Abstract Syntax Tree**, P. Mokri and M. Hempstead, *Boston Area Architecture (BARC) Workshop*, January 2017.

**The Vulnerability of Specialized Architectures to Temperature Side-Channel Information Leakage**, D. Werner, M. Hempstead, K. Juretus, and I. Daulagala, *Boston Area Computer Architecture Workshop (BARC)*, Jan. 2016.

**Fast Multicore Simulation and Performance Analysis of HPC Applications with SynchroTrace**, K. Sangaiah, B. Taskin, and M. Hempstead, *Boston Area Computer Architecture (BARC) Workshop*, January 2016.

**Stockpile Of Accelerators: A Methodology To Increase Accelerators' Coverage**, P. Mokri and M. Hempstead. *Boston Area Computer Architecture (BARC) Workshop*, January 2016.

**Prioritizing Energy Usage by Allocating Inefficiency**, Guru Prasad Srinivasa, Rizwana Begum, M. Hempstead, Geoffrey Challen, *Appears in International Workshop on Mobile Computing Systems and Applications (HotMobile)*, Feb 2014.

**Vertical Arbitration-free 3D NoCs**. A. More, S. Nilakantan, M. Hempstead, B. Taskin. *Proc. Work-In-Progress (WiP) at ACM/IEEE Design Automation Conference (DAC)*, June 2013

**The Case for Power-Agile Computing**, Geoffrey Challen, Mark Hempstead. *USENIX Workshop on Hot Topics in Operating Systems (HotOS)*, May 2011. (**acceptance rate: 25%, citations: 3**)

**An Accelerator-based Wireless Sensor Network Processor in 130nm CMOS**,” Invited paper. Mark Hempstead, Gu-Yeon Wei, and David Brooks. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-09), Grenoble, France, Oct. 2009. (**citations: 12**)

**Navigo: An early-stage model to study power-constrained architectures and specialization** Mark Hempstead, Gu-Yeon Wei and David Brooks. ISCA Workshop on Modeling, Benchmarking, and Simulations (MoBS), June 2009. (**citations: 27**)

**An accelerator-based wireless sensor network processor in 130nm CMOS** Mark Hempstead, Gu-Yeon Wei and David Brooks ISCA Workshop on Architectural Research Prototyping (WARP), June 2009.

**System Design Considerations for Sensor Network Applications (Invited)** Mark Hempstead, Gu-Yeon Wei, and David Brooks. *International Symposium on Circuits and Systems (ISCAS)*. Seattle WA., May 2008. (Invited Session: Energy-Efficient Building Blocks for Ubiquitous Sensing)

**Survey of hardware systems for wireless sensor networks (Invited)** Mark Hempstead, Michael J. Lyons, David Brooks and Gu-Yeon Wei. *ASP Journal of Low Power Electronics*, Vol. 4., No. 1, April 2008. (**citations: 70**)

**Ultra Low Power System Architecture for Wireless Sensor Network Applications** Mark Hempstead, Gu-Yeon Wei, and David Brooks. *Nanoelectronic Devices for Defense & Security Conference (NANO-DDS)*. Washington D.C., June 2007.

**Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications (Design Contest)**, Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, and David Brooks *SRC Student Symposium – SoC design contest Phase 2, 1<sup>st</sup> place*. Raleigh/Durham NC, October 2006.

**Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications (Design Contest)**, Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, and David Brooks *SRC Techcon – SoC design contest Phase 1, 2<sup>nd</sup> place*. Portland, OR, October 2005.

**TinyBench: The Case For A Standardized Benchmark Suite for TinyOS Based Wireless Sensor Network Devices**, Mark Hempstead, David Brooks, and Matt Welsh. *In Proceedings of the First IEEE Workshop on Embedded Networked Sensors (EmNets'04)*, Tampa FL November 2004. (**citations: 27**)

## PUBLIC SOFTWARE RELEASES

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### PRSIM Workload Characterization Tool

A flexible follow on to the Sigil Workload Characterization tool, PRSIM can be connected to a range of front-end instrumentation tools including Valgrind, Dymino Rio, and perf. This allows for the user to write a workload characterization once and then run on different tools.

Published in ISPASS 2018 and released to github March 2018.

<https://github.com/VANDAL/prism>

**“Sigil Workload Profiling Tool for Communication Classification with Binary Instrumentation”** On Git Hub with two major releases so far, 2014 and January 2015. <http://dpac.ece.drexel.edu/current-research-projects/sigil/>. Presented the tool at a public tutorial in conjunction with HPCA 2015, “Research Infrastructures for Accelerator-Centric Architectures” <http://accelerator.eecs.harvard.edu/hpca15tutorial/>

**“SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation”** to be released in Spring 2015 in conjunction with the ISPASS 2015 presentation. There is already interest from ARM, Samsung, and U. Michigan.

## RESEARCH FUNDING

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“Fast and Efficient Hardware Design Exploration through Memory-NoC Analysis for Multi-Core SoCs”  
10/1/2014 – 9/30/2015. **\$100,000**. Samsung GRO program: Next Generation Computing Ultra Low-Power  
Computing For Wearable IoT Devices.

“CSR: Medium: Collaborative Research: Architecture and System Support for Power-Agile Computing.” 8/1/2014  
– 7/31/2018. **\$278,836** (Drexel Portion). National Science Foundation (NSF)

“CAREER: Combating Dark Silicon through Specialization: Communication-Aware Tiled Many-Accelerator  
Architectures” 2/1/2014 – 1/31/2020. **\$470,000**. National Science Foundation (NSF)

“II-NEW: Testbed for High Performance Interconnects” Co-PI (PI is Baris Taskin) 10/1/2013 – 09/31/2018.  
**\$700,000**. National Science Foundation (NSF)

“AfterBurner: Efficient Performance Scaling via Post-Retirement Processing” Subcontract. (PI is Milo Martin)  
1/1/2013 – 8/31/2014. **\$182,996**. University of Pennsylvania and National Science Foundation (NSF).

“Performance Estimation and Optimization of REDHAWK SDR Applications” PI. (Co-PIs Moshe Kam, Kapil  
Dandekar, and Jeremy Johnson) 1/1/2013 – 6/30/3015. Amount and Sponsor Confidential.

“SHF: Small: AfterBurner: Efficient Performance Scaling via Post-Retirement Processing” Co-PI (PI is Amir Roth  
at UPenn) 9/1/2010 – 12/31/2011. **\$118,999** National Science Foundation (NSF).

## PRESENTATIONS AND TALKS

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- 12/2016 “Combating Dark Silicon with Power-Agile Systems and Many-Accelerator Architectures”, Tufts  
University Computer Science Colloquia
- 9/2015 “Combating Dark Silicon: It Takes a Village New Paradigms for Next Generation Power-Aware  
Computing” University at Buffalo
- 3/2015 “Combating Dark Silicon: It Takes a Village New Paradigms for Next Generation Power-Aware  
Computing,” Tufts University
- 2/2015 “Combating Dark Silicon: It Takes a Village New Paradigms for Next Generation Power-Aware  
Computing,” Northeastern University
- 10/2013 Keynote at ICCD Conference. “Combating Dark Silicon: It Takes a Village”. Ashville NC.
- 4/2012 ISPASS FastPath Workshop Invited Speaker “Ultra-Low Power Computing with Accelerator-based  
Architectures“
- 10/2011 “Ultra-Low Power Computing with Accelerator-based Architectures”, Drexel University CS Dept
- 4/2011 “From Sensor Networks to Accelerator-based Architectures” NCSU
- 11/2010 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Swarthmore College
- 9/2010 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Princeton University

- 4/2010 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Washington University, St. Louis
- 7/2009 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, ARM Ltd., Cambridge United Kingdom
- 6/2009 MOBS at ISCA, Austin Texas – “Navigo: An early-stage model to study power-constrained architectures and specialization”
- 6/2009 WARP at ISCA, Austin Texas – “An accelerator-based wireless sensor network processor in 130nm CMOS”
- 6/2009 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, University of Massachusetts Dartmouth
- 4/2009 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Columbia University
- 3/2009 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Bucknell University
- 1/2009 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Drexel University
- 10/2008 “Designing Ultra Low-Power Systems for Wireless Sensor Networks”, Tufts University
- 5/2008 ISCAS Seattle WA – “System Design Considerations for Sensor Network Applications”
- 6/2007 NANO-DDS, Washington DC – “Ultra Low Power System Architecture for Wireless Sensor Network Applications”
- 10/2006 SRC Student Symposium, Raleigh/Durham NC – “Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications”
- 10/2006 CASES, Seoul South Korea – “Architecture and Circuit Techniques for Low-Throughput, Energy-Constrained Systems Across Technology Generations”
- 10/2005 SRC Techcon, Portland OR – “Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications”
- 6/2005 ISCA, Madison WI – “An Ultra Low Power System Architecture for Wireless Sensor Network Applications”

## **CURRENT GRADUATE STUDENTS**

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Cesar Gomes, PhD Candidate, GEM Fellowship Winner (Tufts ECE)  
Alexander Hankin, PhD Student (Tufts ECE)  
Maziar Mehdizadehamiraski, PhD Student (Tufts ECE)  
Parnian Mokri, PhD Candidate (Tufts ECE)  
David Werner, PhD Candidate (Tufts ECE)  
Michael Liu, PhD Candidate Drexel U. (advised by Baris Taskin at Drexel University)  
Karthik Sangaiah, PhD Candidate Drexel U. (advised by Baris Taskin at Drexel University), NSF GREP Fellowship  
Guru Prasad, PhD Candidate U. Buffalo (advised by Geoffery Challen at U. Buffalo/UTUC)



## GRADUATED STUDENTS

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Rizwana Begum, Ph.D, June 2017. Drexel University  
Steven Battle, Ph.D., June 2015. Drexel University  
Siddharth Nilakantan, Ph.D., June 2015. Drexel University

Tomer Shapira, MS 2018, Tufts University (Project Advisor)  
Katia Kravchenko, MS 2018, Tufts University (Project Co-Advisor w/ Ron Lasser)  
Alex Daniels, MS 2017, Tufts University. (Project Advisor)  
Alexander Hankin, MS 2017, Tufts University. (Project Advisor)  
Tara Watson, MS 2017, Tufts University. (Project Advisor)  
Jason Palaszewski, M.S. Drexel University  
Tianyun Zhang, M.S. Drexel University

## UNIVERSITY SERVICE

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2017- Founding Director, MS Program in Computer Engineering (Co-Chair)  
2017- Search Committee Computer Engineering (Chair)  
2017 Lecturer Search Committee (Chair)  
2016- Computer Engineering Curriculum Committee (Chair)  
2016 Tufts School of Engineering OAC Committee Member  
2015 Drexel ECE Senior Design Taskforce Chair  
2015-2014 Graduate Affairs Committee, ECE Department  
2014 Department Chair Search Committee, Electrical and Computer Engineering  
2014-2013 Distinguished Lecture Series in Computer Engineering Organizer  
2013-2011 Computer Engineering Faculty Search Committee  
2015-2011 ECE Senior Design Committee  
2012 Computer Science Faculty Search Committee  
2015-2012 Member of Academic Council and volunteer instructor for Drexel University Computing Academy (DUCA), a five week residential summer program for high school students.  
2010 ECE Department Development Committee

## PROFESSIONAL SERVICE AND REVIEWING ACTIVITY

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### Conference Organization:

1. Local Arrangements Chair, IEEE/ACM International Symposium on Microarchitecture (MICRO) 2017
2. Registration Chair, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2017
3. Technical Program Co-Chair, IEEE International Symposium on Workload Characterization (IISWC) 2016
4. Registration Chair, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015
5. Publications Chair, IEEE International Symposium on Workload Characterization (IISWC) 2014
6. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2014
7. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2013
8. Workshop Organizer, Accelerator Architectures for General-Purpose Computing: from a Hardware, System Software and Application Perspective with HPCA 2012

9. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2012
10. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2011

**Conference Reviewer (Since 2010):**

1. External Review Committee, IEEE International Symposium on Computer Architecture (ISCA), 2019
2. External Review Committee, IEEE International Symposium on High Performance Computer Architecture (HPCA), 2019
3. External Review Committee, IEEE/ACM International Symposium on Microarchitecture (MICRO) 2017
4. Technical Program Committee, 60th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2017
5. External Review Committee, IEEE International Symposium on Computer Architecture (ISCA), 2017
6. External Review Committee, IEEE/ACM International Symposium on Microarchitecture (MICRO) 2016
7. External Review Committee, IEEE International Symposium on High Performance Computer Architecture (HPCA), 2016
8. Program Committee, IEEE International Conference on Computer Design (ICCD) 2015
9. External Review Committee, IEEE/ACM International Symposium on Microarchitecture (MICRO) 2015
10. Program Committee, International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) 2015
11. Program Committee, IEEE International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES 2015).
12. Program Committee, IEEE International Conference on Networking, Architecture, and Storage, (NAS) 2015
13. External Review Committee, IEEE International Symposium on Computer Architecture (ISCA), 2015
14. External Review Committee, IEEE International Symposium on High Performance Computer Architecture (HPCA), 2015
15. Program Committee, International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES) 2014
16. Program Committee, IEEE International Symposium on Workload Characterization (IISWC) 2013
17. Program Committee, Workshop Computer Architecture and Operating System Co-design (CAOS) 2012

**Grant Proposal Panel Reviewer:**

1. 2018 One NSF Panel
2. 2015 One NSF Panel
3. 2014 One NSF Panel
4. 2013 One NSF Panel

**Journal Reviewer (Since 2010):**

1. 2010 ACM Transactions on Sensor Networks
2. 2010 IEEE Transactions on CAD
3. 2010 IEEE Transactions on Computers (ToC)
4. 2010 IEEE Transactions on Wireless Communications
5. 2010 ACM Transactions on Architecture and Code Optimization (TACO)
6. 2011 IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
7. 2011 The International Journal of Computer and Telecommunications Networking (COMNET)
8. 2011 IEEE Transactions on Computers
9. 2011 HPCA Workshop on Architectural Reliability (WRA)
10. 2012 ACM Transactions on Architecture and Code Optimization (TACO)
11. 2012 IEEE Transactions on Computers (ToC)

12. 2013 Computer Architecture Letters (CAL)
13. 2013 IEEE Micro
14. 2013 ACM Transactions on Architecture and Code Optimization (TACO)
15. 2013 IEEE Transactions on Computers (ToC)
16. 2014 ACM Transactions on Architecture and Code Optimization (TACO)
17. 2014 Computer Architecture Letters (CAL)
18. 2015 ASP Journal of Low Power Electronics (JOLPE)
19. 2015 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
20. 2016 ACM Transactions on Architecture and Code Optimization (TACO)
21. 2017 IEEE Transactions on Multi-Scale Computing Systems (TMSCS)
22. 2017 ACM Transactions on Architecture and Code Optimization (TACO)