Proposal for a Timing Model of Ion Trap Quantum Architectures

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ABSTRACT

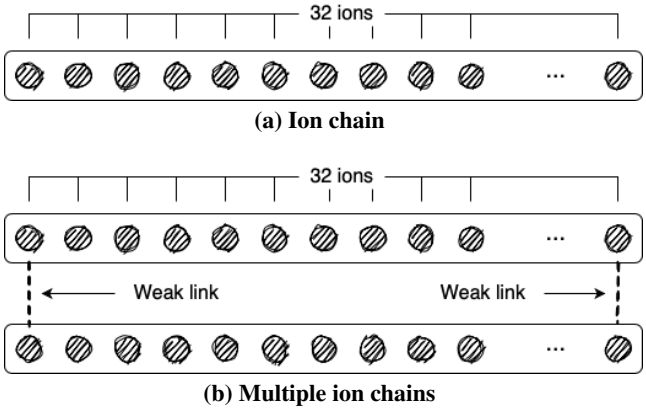
Quantum computers (QCs) have quickly transitioned from the theoretical realm to being physically present in both academic and industry research labs. One of the most promising QC architectures to emerge is the ion trap architecture. Currently, there are no publicly available tools to evaluate the performance (timing) of such architecture which makes it difficult to conjecture about the scalability of the architecture to larger numbers of qubits. In this work, we propose building an open-source software-based timing model of an ion trap QC to evaluate its potential for scalability, especially with respect to performance.

1. INTRODUCTION

As quantum computer (QC) research continues to garner attention, there is an opportunity for architects to innovate alongside physicists. To realize this profound potential, it is crucial for physicists and architects to work together to innovate in such an interdisciplinary area. While architects (generally) do not possess the theoretical physics background required to devise QCs, so do the physicists (generally) not possess the swiss-army-knife-like background of a computer architect in their ability to devise software models to manage the trade-offs in timing, energy, and area, especially as it relates to scalability, across multiple layers of a realistic computing stack.

Currently, multiple flavors of quantum computers exist—those which are based on photons, such as Jiuzhang from USTC [8], and those which are superconductor-based, such as Q System One from IBM [7]. Another version of a QC that has been demonstrated is that referred to as the ion trap QC [1, 3, 4, 5], which is the focus of this work. A high-level overview showing the architecture of a simple ion trap QC is shown in Figure 1. The building block of the ion trap QC is referred to as a chain. This chain contains the trapped ions which act as the qubits which are used for computation. At the moment, the maximum number of ions in a chain is 32. To scale the number of qubits, chains are linked together to form multiple ion chains. Ion trap QCs possess the advantage of providing all-to-all connectivity between qubits within a chain, as well as the condition that all qubit pairs in a chain are equally good. The drawback is connection between multiple chains. This has a longer latency than the links between any two qubits within a chain due to the optics required over free-space paths, which introduces significant drift and noise into the system [2, 6]. We call it a weak link.

The field of tools available to study such devices is sparse. IBM, Microsoft, and Amazon have their respective QC simulators: QisKit, Azure Quantum, and Amazon Braket; however, these are all functional simulators and do not provide crucial information about how the timing scales as a function of the number of 1-qubit and 2-qubit gates. In the case of the ion trap architecture, as far as we are aware there are no publicly available timing models. It is therefore not possible to evaluate the efficacy and promise of this QC architecture. To address this problem, we propose an open-source software-based timing model for the ion trap QC.



(a) Ion chain

(b) Multiple ion chains

Figure 1: Ion trap architecture. Ions are organized in a chain where multiple chains can be linked together. The current physical limit for the number of ions in one chain is 32.

2. METHOD

In this section, we outline our initial proposal of a timing model for the ion trap quantum computer architecture. The model that we propose to build will be implemented using Python and will be designed with three main priorities: flexibility, usability, and extendibility. Further, a user will be able to create batch scripts which will allow for the automated simulation of a large number of ion trap circuits.

2.1 Model parameters

The inputs to the model will be several parameters which give a high level description of a circuit. The model will allow a user to specify any number of 1- and 2-qubit gates as well as an arbitrary circuit depth. To begin with, we will assume that each layer of the quantum circuit is uniform; however, eventually, a user will be able to specify an arbitrary number of different layers. In addition to the circuit depth and total number of gates, the model will contain information about the latency required for different kinds of gates. To

start, all 1-qubit gates will have the same latency, and 2-qubit gates will have one of two latencies depending on if a weak link is involved. The effect of the weak link (in the event of a 2-qubit gate) will be applied randomly using a latency penalty term, α. A summary of the model parameters is displayed in Table 1.

parameter	meaning
q	number of 1-qubit gates
p	number of 2-qubit gates (random qubit pairs)
d	circuit depth
δ	time for 1-qubit gate
γ	time for 2-qubit gate inside chain
$\alpha\gamma$	time for 2-qubit gate between chains

Table 1: Ion trap timing model parameters. The weak link between chains is accounted for by scale factor α.

2.2 Timing expression

For any ion trap quantum circuit specified using the model parameters listed above, we can therefore derive an expression for overall timing, t. This relationship is described in Equation 1. t is a function of both the total latency for 1-qubit and 2-qubit gates as well as the circuit depth. In the case of a 2-qubit gate, there is a possibility of a weak link being present. This is captured by Γ. The expression for Γ is shown in Equation 2. Γ is equivalent to the latency of an arbitrary 2-qubit gate with probability P_{wl} of containing a weak link, where P_{wl} can be derived by considering the number of possible weak links with respect to the total number of 2-qubit combinations in a chain (Equation 3).

$$t \propto d(q\delta + p\Gamma) \tag{1}$$

$$\Gamma \equiv P_{wl}\alpha\gamma + (1 - P_{wl})\gamma \tag{2}$$

$$P_{wl} = \frac{1}{\binom{32}{2} + 1} \tag{3}$$

3. FUTURE GOALS

Now that we have outlined our initial plan for the timing model, in this section we discuss some of the next steps planned in building the model up to a level where it is as useful as possible to the quantum community. First, as previously mentioned, we would like to add support for multiple arbitrary circuit layers rather than the initial model of a d-depth circuit with homogeneous layers. Second, we would like to update our timing model to include specific latency parameters for a wide-range of 1-qubit and 2-qubit gates as it is likely that not all 1-qubit operations will take the same amount of time (likewise for 2-qubit operations). Third, we would like to interface our timing model with an existing functional model of quantum circuits, or, if necessary, implement our own functional model. This is because it is likely that a user will also want to do functional simulation, and so combining these two capabilities into one tool will prevent a user from having to juggle multiple tools.

4. CONCLUSION

We propose an initial methodology for an open-source software-based timing model of an ion trap quantum computer architecture. Using our proposed ion trap timing model, a user will be able to run batch scripts to simulate the effect of weak links on overall circuit timing and how it scales with circuit complexity (number of gates and circuit depth). This is necessary and non-trivial for deep and highly complex quantum circuits. Further, this model will be designed to be easily extended to improve accuracy with real ion trap quantum computers as well as to keep up with the continuously emerging innovations.

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6. STUDENT BACKGROUND

Alexander Hankin is a fourth year PhD candidate in the ECE department at Tufts University under the advisement of Prof. Mark Hempstead. His research interests are centered around architecture-level modeling and simulation. Alex completed the B.S. degree in Computer Engineering with a minor in Mathematics and the M.S. degree in Electrical Engineering in 2017 at Tufts as part of a 5-year combined B.S. and M.S. degree program. Alex has completed research internships at Google and Intel where he has worked on architecture modeling and simulation. Presently, Alex is studying quantum information with Prof. Peter Love and has been investigating ways to apply his classical modeling and simulation background to quantum computing.

REFERENCES

[1] J. Kim, P. Maunz, T. Kim, J. Hussman, R. Noek, A. Mehta, and C. Monroe, "Modular universal scalable ion-trap quantum computer (musiqc)," *AIP Conference Proceedings*, vol. 1363, no. 1, pp. 190–193, 2011. [Online]. Available: https://aip.scitation.org/doi/abs/10.1063/1.3630178

[2] K. K. Mehta, C. Zhang, M. Malinowski, T.-L. Nguyen, M. Stadler, and J. P. Home, "Integrated optical multi-ion quantum logic," *Nature*, vol. 586, no. 7830, p. 533–537, 2020.

[3] C. Monroe and J. Kim, "Scaling the ion trap quantum processor," *Science*, vol. 339, no. 6124, pp. 1164–1169, 2013. [Online]. Available: https://science.sciencemag.org/content/339/6124/1164

[4] C. Monroe, D. M. Meekhof, B. E. King, W. M. Itano, and D. J. Wineland, "Demonstration of a fundamental quantum logic gate," *Phys. Rev. Lett.*, vol. 75, pp. 4714–4717, Dec 1995. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.75.4714

[5] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim, "Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects," *Phys. Rev. A*, vol. 89, p. 022317, Feb 2014. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevA.89.022317

[6] R. J. Niffenegger, J. Stuart, C. Sorace-Agaskar, D. Kharas, S. Bramhavar, C. D. Bruzewicz, W. Loh, R. T. Maxson, R. Mcconnell, D. Reens, and et al., "Integrated multi-wavelength control of an ion qubit," *Nature*, vol. 586, no. 7830, p. 538–542, 2020.

[7] J. Russell, "Ibm quantum update: Q system one launch, new collaborators, and qc center plans," Jan 2019. [Online]. Available: https://www.hpcwire.com/2019/01/10/ibm-quantum-update-q-system-one-launch-new-collaborators-and-qc-center-plans/

[8] H.-S. Zhong, H. Wang, Y.-H. Deng, M.-C. Chen, L.-C. Peng, Y.-H. Luo, J. Qin, D. Wu, X. Ding, Y. Hu, P. Hu, X.-Y. Yang, W.-J. Zhang, H. Li, Y. Li, X. Jiang, L. Gan, G. Yang, L. You, Z. Wang, L. Li, N.-L. Liu, C.-Y. Lu, and J.-W. Pan, "Quantum computational advantage using photons," *Science*, vol. 370, no. 6523, pp. 1460–1463, 2020. [Online]. Available: https://science.sciencemag.org/content/370/6523/1460