Thermal management of microelectronic devices: Challenges and Solutions

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Abstract

Thermal management of microelectronic devices is critical for both functional and long-term reliability of the devices. Unmitigated hotspots significantly limit max performance, increase cost, and degrade reliability. For the last two decades, the thermal community has developed cost effective and efficient technologies to manage the junction temperature of chips while power continues to increase. Thermal interface materials (TIMs) are introduced to reduce interfacial thermal resistance between Silicon chip and its package and between package and heat sink. Figure 1 shows the thermal insulance of state-of-the-art commercial and research laboratory demo TIMs. Innovations in both air cooling and liquid cooling technologies research have pushed the cooling limit to 0.85 W/mm^2 using advanced multi-chip air cooling with integrated vapor chamber, 2.50 W/mm^2 using water cooled separable module level cold plate, 4.6 W/mm^2 with water jet impingement, 7.9 W/mm^2 with micro channels in the device with single phase water flow, and 10.20 W/mm^2 with Micro channels in the device with two-phase for uniform heat flux [5]. Although these cooling technologies show promising thermal performance, there is a long way for their application in industry due to difficulty in manufacturing feasibility, infrastructure and operational cost, and reliability concerns.

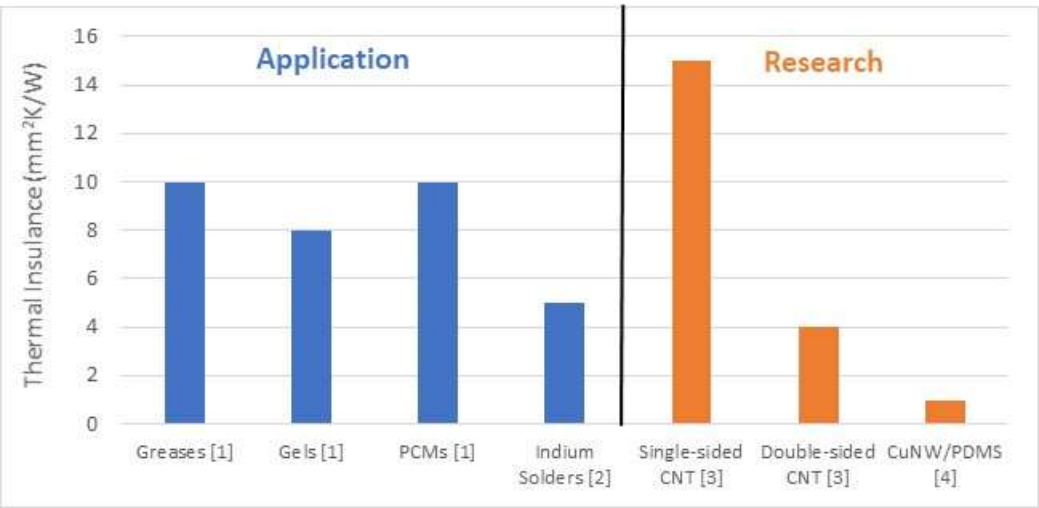

Figure 1 Thermal Resistance of Thermal Interface Materials

Thermal management is facing increasing challenges because of higher power density driven by both performance demand and end of Dennard's scaling. The heat source on chip usually has non-uniform power distribution over the chip area. The nominal thermal demand envelopes

including average power density and hot spot power density shows a trend to continue grow generation over generation for both 2D and 3D package architecture. Heterogeneous on-package integration (2.5D and 3D) of multiple chiplets with diverse IP and Si technology nodes brings additional thermal challenges. High Bandwidth Memory (HBM), as an example of 3D stacked chip, is particularly thermally challenged because of much higher conduction resistance. Hot spots and thermal crosstalk from proximity to high power chips exacerbate the thermal challenges.

These challenges are prevalent in the industry and apply to a broad spectrum of computing products spanning computing, mobile, high-performance graphics, automotive, network infrastructure, and data centers. The Thermal **T**echnical **W**orking **G**roup (TWG), a subchapter of the Heterogeneous Integration Roadmap (HIR) established in 2018, has described these thermal challenges as 7 canonical problems: 2D chip with stacked memory on a silicon/glass interposer, 3D stacked die with conduction interfaces, 3D stacked die with embedded liquid cooling, optics/photonics based Heterogeneous package, harsh environment (military, aerospace, automobile), mobile application chipset (package on package, fan out, bridge), and voltage Regulators in a Heterogenous Package.

To solve these challenges, we need a holistic approach which consists of - but is not limited to - understanding transient workload-thermal behavior, architecture, and microarchitecture choice to monitor and proactively mitigate transient power, and optimizing physical design (e.g., floor planning and power density aware) to address heat source issue. In the meanwhile, advanced packaging technology needs to improve package thermal performance with new package architecture, material, and manufacturing process development, while thermal community continues innovation in cooling solutions and system design. It's also critical to develop tools and frameworks to study the cross-stack thermal hotspot problem to identify solutions.

References

1. Prasher, R. (2006). Thermal Interface Materials: Historical Perspective, Status, and Future Directions. *Proceedings of the IEEE 94.8*, 1571-1586.
2. Vijay, K. (2012). Solder-TIMs (Thermal Interface Materials) for Superior Thermal Management in Power Electronics. *4th Electronic System-Integration Technology Conference* (pp. 1-5). Brighton: IEEE.
3. Baratunde A. Cola, J. X. (2007). Photoacoustic characterization of carbon nanotube array thermal interfaces. *Journal of Applied Physics 101 (5)*, 054313.
4. Michael T. Barako, S. G. (2017). "Dense vertically aligned copper nanowire composites as high performance thermal interface materials. *ACS applied materials & interfaces, 9(48)*, 42067-42074.
5. Thermal Chapter 2021 publication, HIR, IEEE.